WD1100 Series Winchester Controller Chips

DESCRIPTION

The WD1100 Chip series provides a low cost alternative for developing a Winchester Controller. These devices have been designed to read and convert an MFM data stream into 8-bit parallel bytes. During a write operation, parallel data is converted back into MFM to be written on the disk. Address Marks are generated and detected while CRC bytes can be appended and checked on the data stream. The WD1100 is fabricated in N-channel silicon gate technology and is available in a 20-pin Dual-In-Line package.

- WD1100-01 SER/PARALLEL CONVERTER
- WD1100-02 MFM GENERATOR
- WD1100-12 IMPROVED MFM GENERATOR
- WD1100-03 AM DETECTOR
- WD1100-04 CRC GENERATOR/CHECKER
- WD1100-05 PAR/SERIAL CONVERTER
- WD1100-06 ECC/CRC LOGIC
- WD1100-07 HOST INTERFACE LOGIC
- WD1100-09 DATA SEPARATION SUPPORT LOGIC

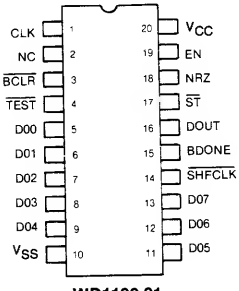
FEATURES

- SA1000/ST506 COMPATIBLE
- SINGLE 5V SUPPLY
- TRI-STATE DATA LINES
- 5 MBITS/SEC TRANSFER RATE
- SIMPLIFIED INTERCONNECT

APPLICATIONS

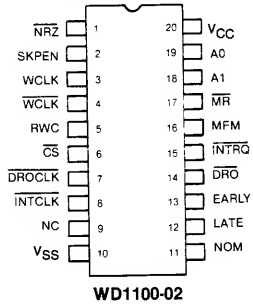
Winchester Controllers For:

- SHUGART ASSOCIATES
- SEAGATE TECHNOLOGY
- QUANTUM CORP.
- TANDON MAGNETICS
- MINISCRIBE
- RMS
- CMI . . . AND OTHERS



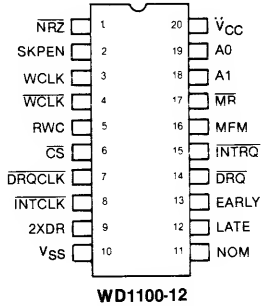
WD1100-01

SERIAL/PARALLEL CONVERTER



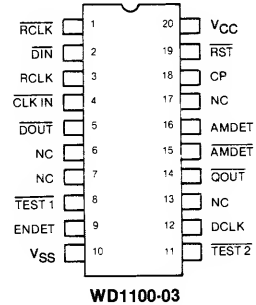
WD1100-02

MFM GENERATOR



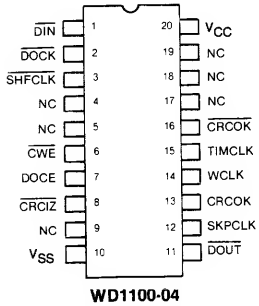
WD1100-12

IMPROVED MFM GENERATOR



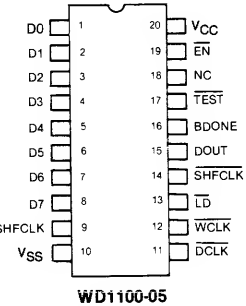
WD1100-03

AM DETECTOR



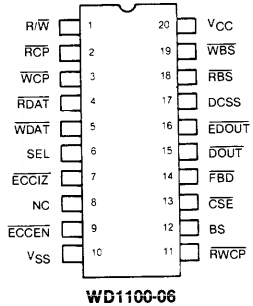
WD1100-04

CRC GENERATOR/CHECKER



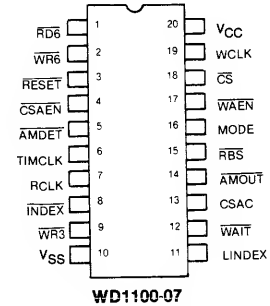
WD1100-05

PARALLEL/SERIAL CONVERTER



WD1100-06

ECC/CRC LOGIC



WD1100-07

HOST INTERFACE LOGIC

See page 481 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-01 Serial/Parallel Converter

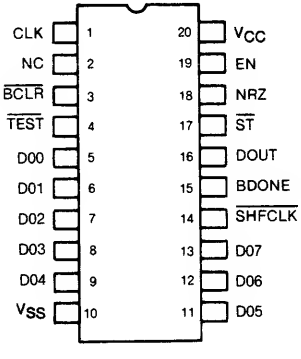
DESCRIPTION

The WD1100-01 Serial/Parallel Converter allows the user to convert NRZ (non-return to zero) data from a Winchester disk drive into 8 bit parallel form. Additional inputs are provided to signal the start of the parallel process, as well as Byte Strobes to signify the end of the conversion. The device contains two sets of 8-bit registers; one register may be read (in parallel), while data is being shifted into the other register. This double-buffering allows the Host to read data from the disk drive at one-eighth the actual data rate.

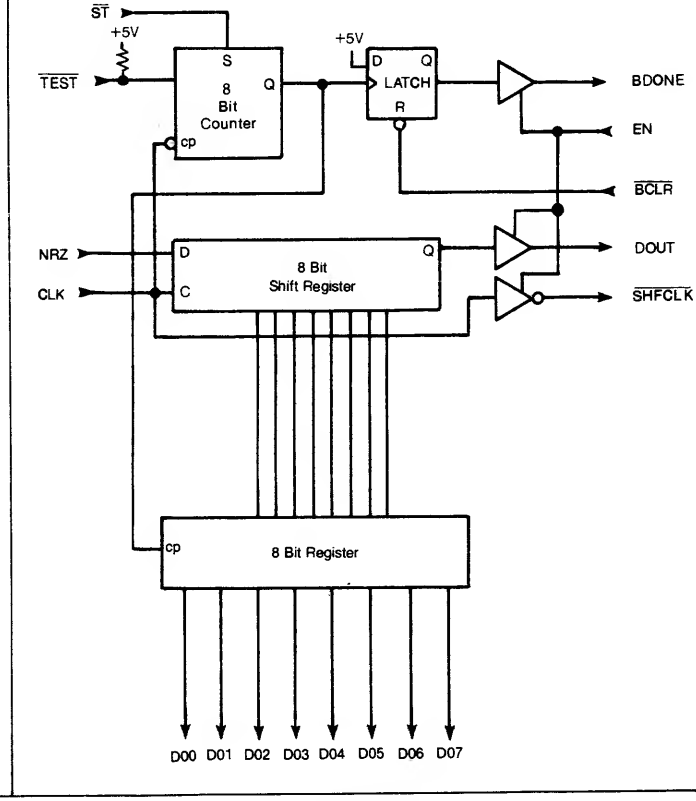
The WD1100-01 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5MBITS/SEC SHIFT RATE
- SERIAL IN/SERIAL-PARALLEL OUT
- 20 PIN DIP PACKAGE



WD1100-01
Figure 1. Pin Connections



WD1100-01
Figure 2. Block Diagrams

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	CLK	CLOCK	NRZ data is entered into the 8-bit shift register on the low-to-high transition of clock.
2	NC	NO CONNECTION	No connection. This pin is to be left open by the user.
3	$\overline{BCLR}$	$\overline{BYTE\ CLEAR}$	When this line is at a logic 0, the BDONE (Pin 15) line is held reset.
4	$\overline{TEST}$	$\overline{TEST\ INPUT}$	This pin must be left open by the user.
5-9, 11-13	D00-D07	DATA0-DATA7	8 bit parallel data outputs.
10	V_{SS}	GROUND	Ground.
14	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	Inverted copy of CLOCK (pin 1) which is active when EN (pin 19) is at a logic 1.
15	BDONE	BYTE DONE	This signal is forced to a logic 1 signifying 8 bits of data have been assembled. BDONE remains in a logic 1 state until reset by a logic 0 on the BCLR (pin 3) line.
16	DOUT	DATA OUT	Serial Data Output from the 8th stage of the internal shift register. DOUT is in a high impedance state whenever EN (pin 19) is at a logic 0.
17	$\overline{ST}$	$\overline{START}$	This line enables the byte counter and is used for synchronization. It must be held to a logic 1 prior to first data bit on the NRZ (Pin 18) line.
18	NRZ	NRZ DATA	NRZ serial data is entered on this pin and clocked by the low to high transition of CLK (pin 1).
19	EN	ENABLE	When this signal is at a logic 0, DOUT, $\overline{SHFCLK}$, and BDONE outputs are in a high impedance state.
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the WD1100-01 must be synchronized to the data stream. The $\overline{ST}$ line (Pin 17 high) is used to hold the internal bit counter in a cleared state until valid data (NRZ) and clocks (CLK) are entered. The $\overline{ST}$ line is a synchronous input and therefore requires one full cycle of the CLK line (Pin 1) to occur in order to accept a $\overline{ST}$ condition. After this happens, the device is ready to perform serial to parallel conversions.

Data is entered on the NRZ line and clocked into the 8-bit shift register on the low-to-high transition of CLK. The $\overline{ST}$ line must be set low during the low time of CLK. Data is accepted on low-to-high transition of the clock while the high-to-low transition of CLK increments the bit counter. After 8 data bits have been entered the final high-to-low transition of CLK sets an internal latch tied to the BDONE line (Pin 15). At the same time, the contents of the shift register are parallel loaded into an 8 bit register making the parallel data available on the D00-D07 outputs. BDONE will remain in a latched state until the $\overline{BCLR}$ is set to a logic 0, clearing off the BDONE signal. $\overline{BCLR}$ is a level triggered input and must be set back to a logic 1 before the next 8 bits are shifted through the register. BCLR has no effect on the serial shifting process. When the next 8 bits are received, BDONE will again be set and the operation continues.

When interfacing to a microprocessor, BDONE is used to indicate a parallel byte is ready to be read. As the processor reads the data out of the D00-D07 lines, the $\overline{BCLR}$ line should be strobed to clear off BDONE in anticipation of the next assembled byte. An address decode signal generated at the host may be used for this purpose. During a power-up condition, the state of BDONE is indeterminant. It is recommended that $\overline{BCLR}$ be strobed low after power-up to insure that BDONE is cleared.

The serial output line from the last stage of the shift register is available on the DOUT pin. An inverted copy of CLK is available on the $\overline{SHFCLK}$ pin. Both DOUT (Pin 16) and $\overline{SHFCLK}$ (Pin 14) can be used to drive another shift register external to the device.

The three signals BDONE, DOUT, and $\overline{SHFCLK}$ can be placed in a high impedance state by setting EN (Pin 19) to a logic 0. Likewise, EN must be at a logic 1 in order for these signals to be active.

The $\overline{TEST}$ pin is internally OR'ed with the $\overline{ST}$ line to inhibit the bit counter. It is recommended that $\overline{TEST}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required internally for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... 0°C to 50°C
Voltage on any pin
with respect to V_{SS} ..... −0.2V to +7.0V
Power Dissipation..... 1 Watt
STORAGE TEMPERATURE
PLASTIC..... −55°C to +125°C
CERAMIC..... −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

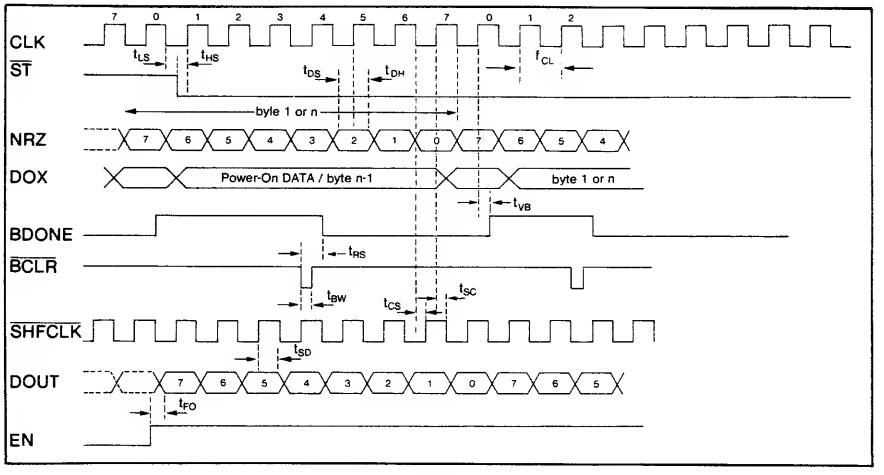
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_O	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC Electrical Characteristics T_A = 0° to 50°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNITS	CONDITION
f_{CL}	CLK FREQUENCY	0		5.25	MHZ	
t_{LS}	↓CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{HS}	↑CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{DS}	Data set-up to ↑CLK	15			nsec	
t_{VB}	BDONE valid from ↑CLK	65		110	nsec	EN = 1
t_{RS}	BDONE reset from $\overline{BCLR}$			110	nsec	EN = 1
t_{BW}	$\overline{BCLR}$ Pulse Width	50			nsec	EN = 1
t_{SC}	↑CLK to ↓$\overline{SHFCLK}$			90	nsec	EN = 1
t_{CS}	↓CLK to ↑$\overline{SHFCLK}$			100	nsec	EN = 1
t_{SD}	Data delay from ↑$\overline{SHFCLK}$			55	nsec	EN = 1
t_{FO}	Enable to DOUT ACTIVE			90	nsec	
t_{DH}	Data Hold w.r.t. ↑CLK	25			nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-01
Figure 3.

See page 481 for ordering information.

Western Digital
WD1100-02 MFM Generator

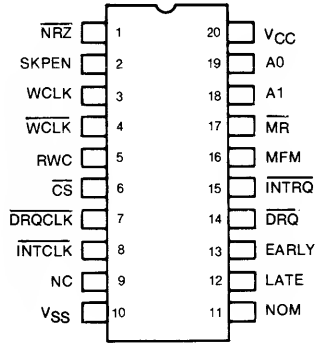
DESCRIPTION

The WD1100-02 MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-02 is the ability to delete a clock pulse in the outgoing MFM stream in order to record Address Marks.

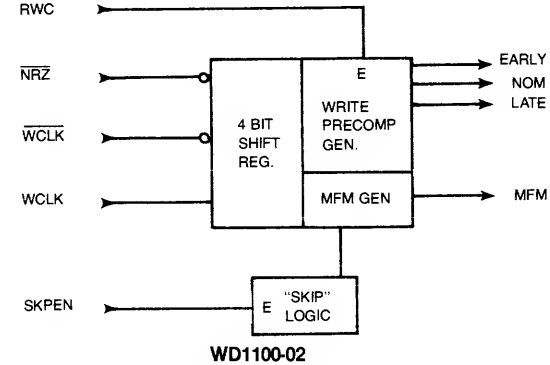
The WD1100-02 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

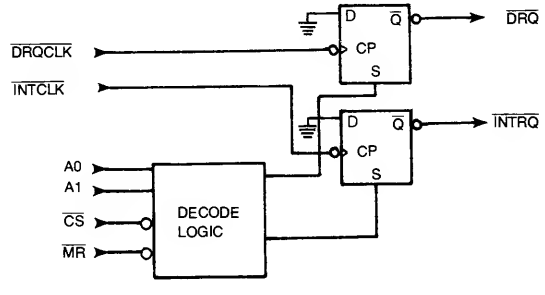
- SINGLE + 5V SUPPLY
- 5 M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION
- 20 PIN DIP PACKAGE



WD1100-02
Figure 1. Pin Connections



WD1100-02
Figure 2. Block Diagram MFM Generator



WD1100-02
Figure 3. Block Diagram Interrupt Control Logic

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	NON-RETURN-TO ZERO	NRZ data input that is strobed into the MFM generator by WCLK (↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3).
4	$\overline{WCLK}$	WRITE CLOCK	
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	NC	No Connection	No Connection.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing.
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	CHIP SELECT	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	INTERRUPT REQUEST CLOCK	A high-to-low transition on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	DATA REQUEST CLOCK	A high-to-low transition on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	INTERRUPT REQUEST	This output is latched at a logic 0 when INTCLK (pin 8) makes a high-to-low transition while the decode logic is disabled.
14	$\overline{DRQ}$	DATA REQUEST	This output is latched at a logic 0 when DRQCLK (pin 7) makes a high-to-low transition while the decode logic is disabled.
17	$\overline{MR}$	MASTER RESET	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18, 19	A_0,A_1	ADDRESS 1, 0	When CS is low and the address lines are high, INTRQ is cleared; if the address lines are low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ±10% power supply input.

DEVICE DESCRIPTION

The WD1100-02 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the $\overline{NRZ}$ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1. The algorithm used is on Page 8.

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using $A1_{16}$ data with $0A_{16}$ clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the $\overline{NRZ}$ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data patterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

$\overline{MR}$	A_1	A_0	$\overline{CS}$	$\overline{DRQ}$	$\overline{INTRQ}$
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q_N

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only on the high-to-low transition of $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°c to 50°c
Voltage on any pin with respect to V_{SS} . . −0.2V to + 7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE:
PLASTIC . . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C, V_{CC} = +5V ± 10%, V_{SS} = 0V

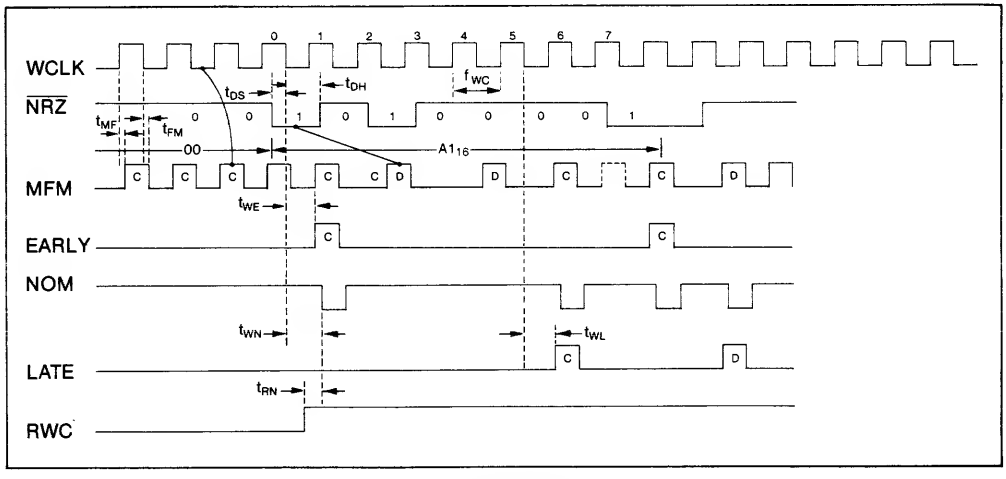
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{OC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

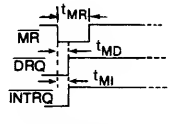
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t. ↓WCLK	10			nsec	
t_{DH}	Data hold w.r.t. ↓WCLK	25			nsec	
t_{MF}	↑WCLK to ↑MFM delay			160	nsec	Pin 1 LOW
t_{FM}	↓WCLK to ↓MFM delay			180	nsec	Pin 1 LOW
t_{WN}	Data delay to NOM from ↓WCLK			190	nsec	Pin 4 = LOW
t_{WE}	Data delay to EARLY from ↓WCLK			180	nsec	Pin 4 = LOW
t_{WL}	Data delay to LATE from ↓WCLK			180	nsec	Pin 4 = LOW
t_{MR}	Master reset pulse width	50			nsec	
t_{MD}	↓$\overline{MR}$ to ↑$\overline{DRQ}$			150	nsec	

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑ $\overline{INTRQ}$			150	nsec	
t_{DQ}	$\overline{DRQCLK}$ pulse width	50			nsec	
t_{IQ}	$\overline{INTCLK}$ pulse width	50			nsec	
t_{DD}	↓ $\overline{DRQCLK}$ to $\overline{DRQ}$			120	nsec	
t_{II}	↓ $\overline{INTCLK}$ to $\overline{INTRQ}$			120	nsec	
t_{AD}	↓AX to ↑ $\overline{DRQ}$			145	nsec	
t_{AI}	↑AX to ↑ $\overline{INTRQ}$			160	nsec	
t_{CD}	↓ $\overline{CS}$ to ↑ $\overline{DRQ}$			145	nsec	
t_{CI}	↓ $\overline{CS}$ to ↑ $\overline{INTRQ}$			180	nsec	
t_{RN}	↑RWC to ↓NOM			115	nsec	

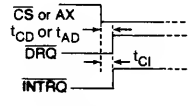
NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V.



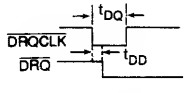
WD1100-02
Figure 4. MFM Generator Timing



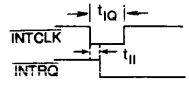
WD1100-02
Figure 5



WD1100-02
Figure 6



WD1100-02
Figure 7.



WD1100-02
Figure 8.

See page 481 for ordering information.

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Western Digital
WD1100-12 Improved MFM Generator

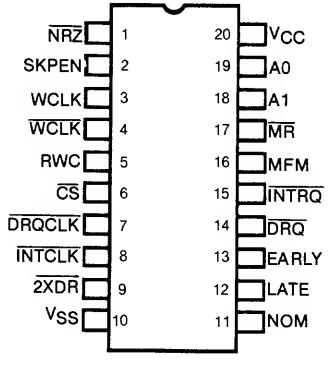
DESCRIPTION

The WD1100-12 improved MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-12 is the ability to delete a clock pulse in the outgoing MFM stream-in order to record Address Marks.

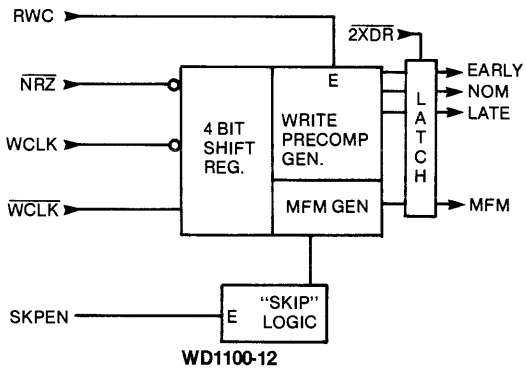
The WD1100-12 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

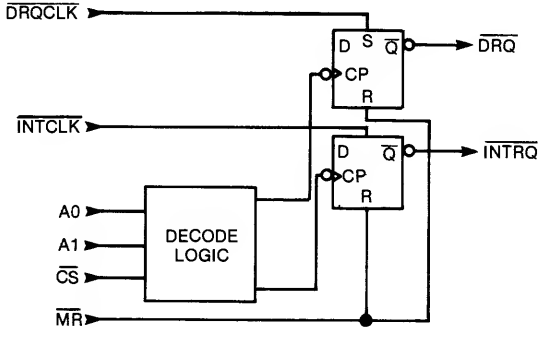
- SINGLE +5V SUPPLY
- 5 M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION



WD1100-12
Figure 1. Pin Connections



WD1100-12
Figure 2. Block Diagram MFM Generator



WD1100-12
Figure 3. Block Diagram Interrupt Control Logic

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	NON-RETURN-TO ZERO	NRZ data input that is strobed into the MFM generator by WCLK(↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3).
4	$\overline{WCLK}$	WRITE CLOCK	
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	$\overline{2XDR}$	2 TIMES DATA RATE	This input is used to latch EARLY, LATE, NOM and MFM outputs.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing.
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	CHIP SELECT	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	INTERRUPT REQUEST CLOCK	A low on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	DATA REQUEST CLOCK	A low on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	INTERRUPT REQUEST	This output is latched at a logic 0 when INTCLK (pin 8) goes/ is low.
14	$\overline{DRQ}$	DATA REQUEST	This output is latched at a logic 0 when DRQCLK (pin 7) goes/is low.
17	$\overline{MR}$	MASTER RESET	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18, 19	A_0,A_1	ADDRESS 0, 1	When CS is low and the address lines go high, INTRQ is cleared; if the address lines go low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

The WD1100-12 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the $\overline{NRZ}$ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1. The algorithm used is on Page 4.

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using $A1_{16}$ data with $0A_{16}$ clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the NRZ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data patterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

MR	A_1	A_0	CS	DRQ	INTRQ
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q_N

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only by a low level or $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias..... 0°C to 50°C
Voltage on any pin with respect to V_{SS} ... −0.2V to +7.0V
Power Dissipation..... 1 Watt

STORAGE TEMPERATURE:
PLASTIC..... −55°C to +125°C
CERAMIC..... −55°C to +150°C

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

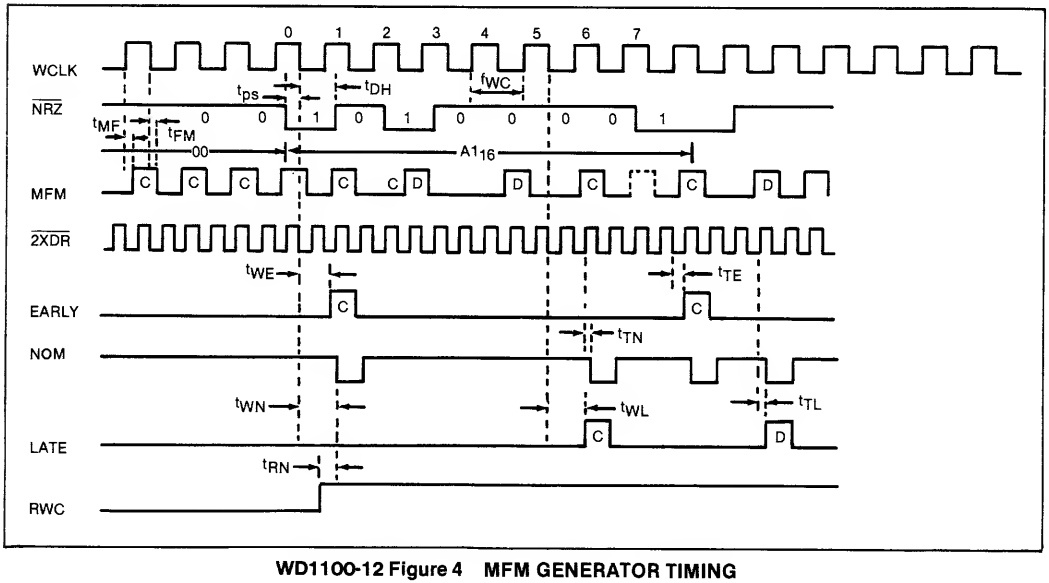
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

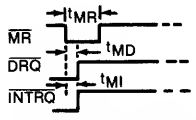
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{FR}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t. ↓WCLK	10			nsec	
t_{DH}	Data hold w.r.t. ↓WCLK	25			nsec	
t_{MF}	↑WCLK to ↑MFM delay			210	nsec	Pin 1 LOW
t_{FM}	↓WCLK to ↓MFM delay			230	nsec	Pin 1 LOW
t_{WN}	Data delay to NOM from ↓WCLK			240	nsec	
t_{WE}	Data delay to EARLY from ↓WCLK			230	nsec	
t_{WL}	Data delay to LATE from ↓WCLK			230	nsec	
t_{MR}	Master reset pulse width	50			nsec	
t_{MD}	↓$\overline{MR}$ to ↑$\overline{DRQ}$			150	nsec	

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑$\overline{INTRQ}$			150	nsec	
t_{DQ}	$\overline{DRQCLK}$ pulse width	50			nsec	
t_{IQ}	$\overline{INTCLK}$ pulse width	50			nsec	
t_{DD}	↓$\overline{DRQCLK}$ to $\overline{DRQ}$			120	nsec	
t_{II}	↓$\overline{INTCLK}$ to $\overline{INTRQ}$			120	nsec	
t_{AD}	↓AX to ↑$\overline{DRQ}$			145	nsec	
t_{AI}	↑AX to ↑$\overline{INTRQ}$			160	nsec	
t_{CD}	↓$\overline{CS}$ to ↑$\overline{DRQ}$			145	nsec	
t_{CI}	↓$\overline{CS}$ to ↑$\overline{INTRQ}$			180	nsec	
t_{RN}	↑RWC to ↓NOM			145	nsec	
t_{TE}	↓$\overline{2XDR}$ to ↑EARLY			75	nsec	
t_{TN}	↓$\overline{2XDR}$ to ↑NOM			75	nsec	
t_{TL}	↓$\overline{2XDR}$ to ↑LATE			75	nsec	

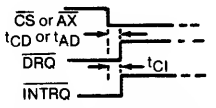
NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V.



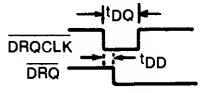
WD1100-12 Figure 4 MFM GENERATOR TIMING



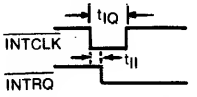
WD1100-12 Figure 5



WD1100-12 Figure 6



WD1100-12 Figure 7



WD1100-12 Figure 8

See page 481 for ordering information.

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Western Digital
WD1100-03 AM Detector

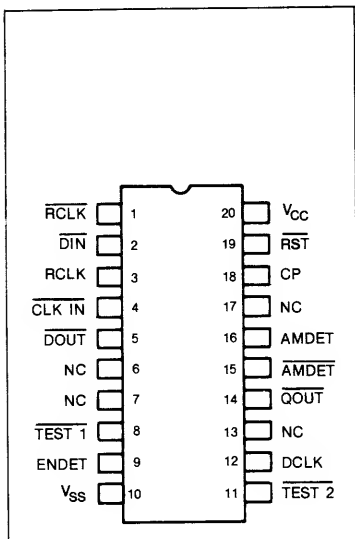
DESCRIPTION

The WD1100-03 Address Mark Detector provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM (NRZ) clocks and data are fed to the device along with a window clock generated by an external data separator. The WD1100-03 searches the data stream for a DATA = A1, CLK = 0A pattern and produces an AM DET signal when the pattern has been found. NRZ data is an output from the device, which can be used to drive a serial/parallel converter. An uncommitted latch is also provided for by the data separator circuitry, if required.

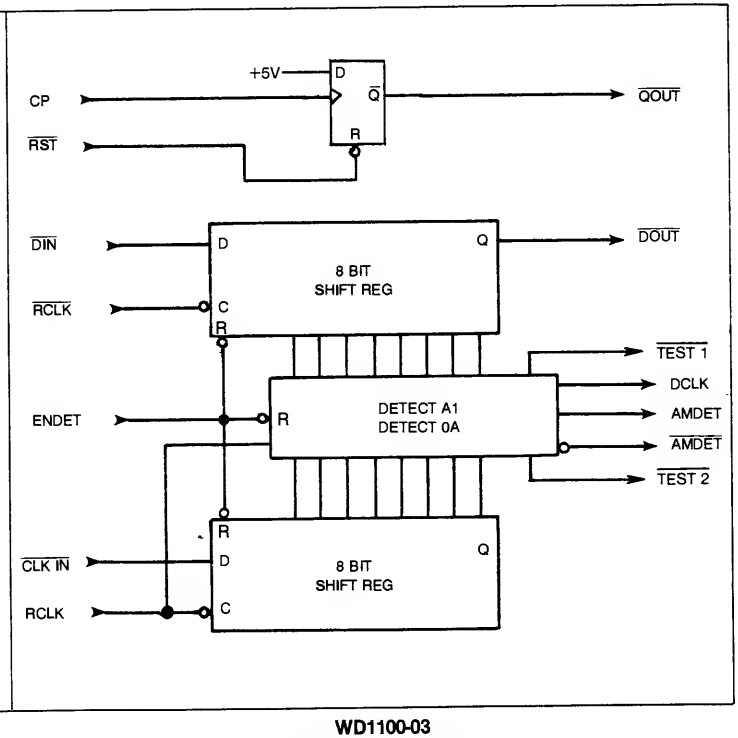
The WD1100-03 Address Mark Detector is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- 5 MBITS/SEC DATA RATE
- DECODES $A1_{16}$-$0A_{16}$
- SYNCHRONOUS CLOCK/DATA OUTPUTS
- 20 PIN DIP PACKAGE



WD1100-03
Figure 1. Pin Connections



WD1100-03
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1 3	$\overline{\text{RCLK}}$ RCLK	$\overline{\text{READ CLOCK}}$ READ CLOCK	Complimentary clock inputs used to clock DIN and $\overline{\text{CLK}}$ IN into the AM detector.
2	$\overline{\text{DIN}}$	$\overline{\text{DATA INPUT}}$	MFM data pulses from the external Data Separator are connected on this line.
4	$\overline{\text{CLK IN}}$	$\overline{\text{CLOCK INPUT}}$	MFM clock pulses from the external Data Separator are connected on this line.
5	$\overline{\text{DOUT}}$	$\overline{\text{DATA OUTPUT}}$	Data Output from the internal Data Shift register, synchronized with DCLK.
6, 7, 13, 17	NC	No Connection	To be left open by the user
8 11	$\overline{\text{TEST 1}}$ $\overline{\text{TEST 2}}$	$\overline{\text{TEST 1}}$ $\overline{\text{TEST 2}}$	To be left open by the user.
9	ENDET	ENABLE DETECTION	A logic 1 on this line enables the detection logic to search for a data $A1_{16}$ and clock.
10	V_{SS}	V_{SS}	GROUND.
12	DCLK	DATA CLOCK	Clock output that is synchronized with $\overline{\text{DATA OUT}}$ (Pin 5).
14	$\overline{\text{QOUT}}$	$\overline{\text{LATCH OUTPUT}}$	Signal output from the uncommitted latch.
15	$\overline{\text{AMDET}}$	$\overline{\text{ADDRESS MARK DETECT}}$	Complimentary Address Mark Detector output. These signals will go active when a Data = $A1_{16}$ Clock = $0A_{16}$ pattern is detected in the data stream.
16	AMDET	ADDRESS MARK DETECT	
18	CP	CLOCK PULSE	A low-to-high transition on this line will cause the $\overline{\text{QOUT}}$ (Pin 14) to be latched at a logic 0.
19	$\overline{\text{RST}}$	$\overline{\text{RESET}}$	A logic 0 on this line will cause the QOUT (Pin 14) signal to be set at a logic 1.
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the internal logic must be initialized. While the ENDET (Pin 9) line is at a logic 0, shifting of data will be inhibited and $\overline{\text{AMDET}}$, AMDET, $\overline{\text{CLK}}$, and $\overline{\text{DATA OUT}}$ will remain inactive.

When ENDET is at a logic 1, shifting is enabled. NRZ data is entered on the $\overline{\text{DIN}}$ line (Pin 2) and shifted on the high-to-low transition of $\overline{\text{RCLK}}$ (Pin 1). NRZ clocks are entered on the $\overline{\text{CLK}}$ IN line, and shifted on the high-to-low transition of RCLK (Pin 3). The $\overline{\text{DOUT}}$ line (Pin 5) is tied to the last stage of the internal Data Shift register and will reflect information clocked into the DIN line delayed by 8 bits.

While each bit is being shifted, a 16 bit comparator is continuously checking the parallel contents of the shift registers for the DATA = $A1_{16}$, CLK = $0A_{16}$ pattern. When this pattern is detected, AMDET will be set to a logic 0 and AMDET will be set to a logic 1. $\overline{\text{AMDET}}$ and AMDET will remain latched until the device is re-initialized by forcing ENDET to a logic 0.

When an AM is detected, DCLK will begin to toggle. Data present on the $\overline{\text{DOUT}}$ line may then be clocked into an external serial/parallel converter. DCLK will remain inactive when ENDET is held at a logic 0.

An uncommitted edge-triggered flip/flop has been provided to facilitate the detection of high frequency by the data separator, but may be used for any purpose. The low-to-high transition of CP (Pin 18) will set the $\overline{\text{QOUT}}$ (Pin 14) to a logic 0. $\overline{\text{QOUT}}$ may be reset back to a logic 1 by a low level on the $\overline{\text{RST}}$ line (Pin 19).

$\overline{\text{TEST1}}$ and $\overline{\text{TEST2}}$ are output lines. $\overline{\text{TEST1}}$ is an active low pulse when an $A1_{16}$ is detected, and $\overline{\text{TEST2}}$ is active low pulse when a $0A_{16}$ is detected. These signals are used for test points and therefore should be left open by the user if not required.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias ..... 0°C to 50°C
Voltage on any pin with respect to V_{SS} ... −0.2V to +7.0V
Power dissipation ..... 1 Watt

STORAGE TEMPERATURE
PLASTIC ..... −55°C to +125°C
CERAMIC ..... −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

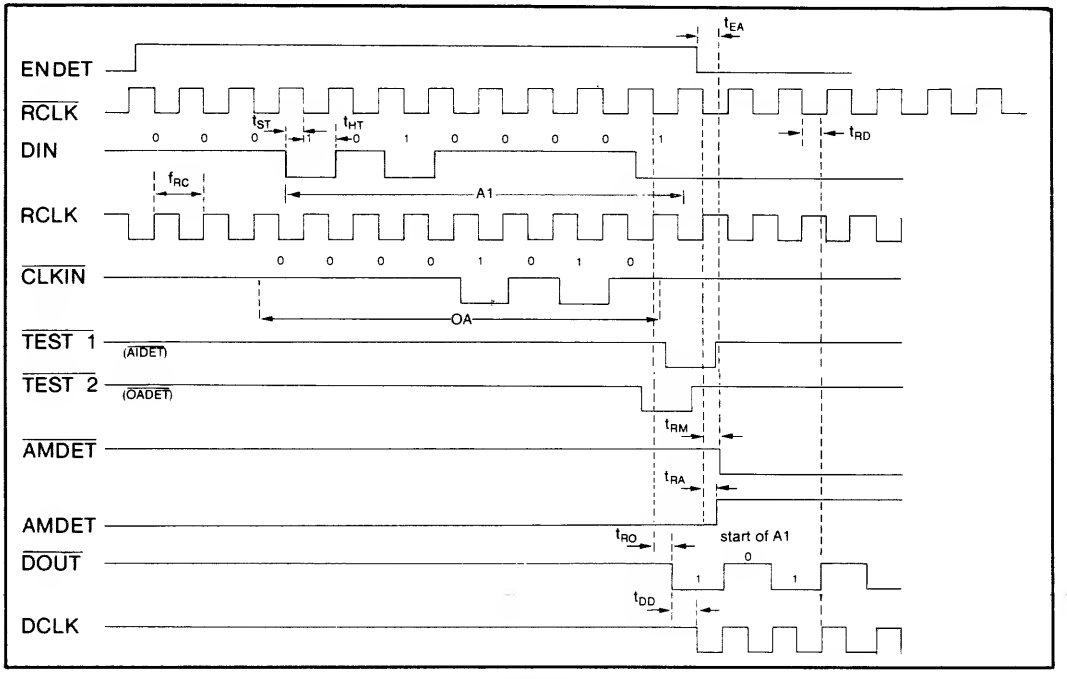
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.7	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{RC}	RCLK Frequency			5.25	MHZ	
t_{ST}	Data Setup time	40			nsec	
t_{HT}	Data Hold time	10			nsec	
t_{DD}	$\overline{DOUT}$ to DCLK DELAY			110	nsec	
t_{RD}	↓$\overline{RCLK}$ to ↑ DCLK			120	nsec	
t_{RA}	↓$\overline{RCLK}$ to ↑ AMDET			115	nsec	
t_{RM}	↓$\overline{RCLK}$ to ↓ $\overline{AMDET}$			125	nsec	
t_{RO}	↓$\overline{RCLK}$ to $\overline{DOUT}$			135	nsec	
t_{EA}	↓ENDET to ↓AMDET			130	nsec	
t_{RQ}	↓$\overline{RST}$ to ↑ $\overline{QOUT}$			110	nsec	
t_{RW}	Pulse width of $\overline{RST}$	50			nsec	
t_{CW}	CP Pulse width	90			nsec	
t_{CQ}	↑CP to ↓ $\overline{QOUT}$			106	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5V.



WD1100-03
Figure 3. Functional Timing

See page 481 for ordering information.

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Western Digital
WD1100-04 CRC Generator/Checker

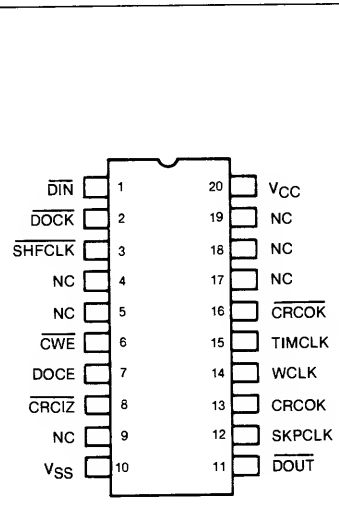
DESCRIPTION

The WD1100-04 CRC Generator/Checker is designed to generate a Cyclic Redundancy Checkword from a serial data stream, and to check a data stream against a known CRC word. Complimentary latched "CRCOK" outputs are provided to indicate CRC errors in check mode. Additional logic has been included to shift the CRC checkword out of the device by signals generated on other WD1100 family devices.

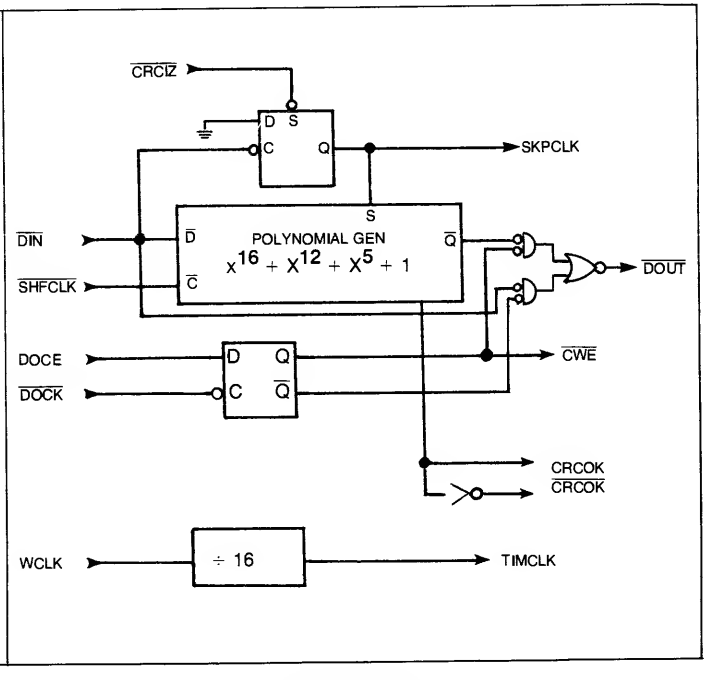
The WD1100-04 is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- GENERATES/CHECKS CRC
- SINGLE + 5V SUPPLY
- LATCHED ERROR OUTPUTS
- $X^{16} + X^{12} + X^5 + 1$ (CCITT-16)
- AUTOMATIC PRESET
- 20 PIN DIP PACKAGE



WD1100-04
Figure 1. Pin Connections



WD1100-04
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{DIN}$	$\overline{DATA\ INPUT}$	Active low serial input data stream is used to generate/check the 2 byte CRC word.
2	$\overline{DOCK}$	$\overline{DATA\ OR\ CRC\ WORD\ CLOCK}$	After a byte of data has been transferred in, this input signal is used to latch the state of DOCE in an internal D flop with a high to low transition.
3	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	The falling edge shifts data bits into the CRC generator/checker. It also transfers the CRC check word to $\overline{DOUT}$ in the write mode (DOCE = LOW). The rising edge also activates the CRCOK lines in the read mode when no error is found.
4, 5	N.C.	NO CONNECTION	
6	$\overline{CWE}$	$\overline{CHECK\ WORD\ ENABLE}$	This active low output indicates that the CRC checkword is being output on the $\overline{DOUT}$ line. When $\overline{CWE}$ is high, data is being output on $\overline{DOUT}$.
7	DOCE	DATA OR CRC ENABLE	Initially, this input line is held high to direct input data (pin 1) to the output data (pin 11). After the next to the last BYTE is transmitted but before the last BYTE occurs DOCE must be low to direct the 2 CRC check bytes to DOUT (pin 11). DOCE must be maintained low for a minimum of 2 byte times. DOCE is used only in the write mode.
8	$\overline{CRCIZ}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ INITIALIZE}$	When this line is at a logic 0, the SKPCLK output line is held high and the CRC generator is held preset to hex "FFFF."
9	N.C.	NO CONNECTION	
10	V_{SS}	GROUND	GROUND.
11	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	In the write mode, this line outputs the unmodified data stream along with the 2 byte CRC word appended to the end of the stream.
12	SKPCLK	SKIP CLOCK	The first high-to-low transition on $\overline{DIN}$ (pin 1) resets SKPCLK low and enables the CRC to either generate or check the CRC word.
13	CRCOK	CYCLIC REDUNDANCY CHECK OKAY	In the read mode, after the 2 byte CRC word is entered on $\overline{DIN}$ and no error has been detected, this line is set high to indicate no errors have occurred. This line will then remain high as long as $\overline{DIN}$ is maintained high.
14	WCLK	WRITE CLOCK	This input clock is divided by 16 to produce TIMCLK (pin 15) and has no effect on the rest of the internal circuitry.
15	TIMCLK	TIMING CLOCK	See above.
16	$\overline{CRCOK}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ OKAY}$	Complementary output version of CRCOK (pin 13).
17-19	N.C.	NO CONNECTION	
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data thru the device (either in the read or write modes) the CRC generator/checker is initialized by strobing the $\overline{CRCIZ}$ (pin 8) low. This forces the SKPCLK (pin 12) line to the high state. The first low going transition on $\overline{DIN}$ (pin 1), namely the most significant bit of an address mark, resets the SKPCLK line. The WD1100-04 has now been properly initialized and is ready to generate/check the CRC bytes. The CRCOK and $\overline{CRCOK}$ lines should be set to their inactive states.

In the write mode, initially the DOCE (pin 7) is held high and a pseudo $\overline{DOCK}$ is produced by supplying a string of zeros before the address mark. This ensures the proper state of the internal D flip flop to gate input data to the output line $\overline{DOUT}$ (pin 11). As shown in the block diagram the $\overline{CWE}$ (pin 6) will be set high. Sometime between the next to the last and the last $\overline{DOCK}$ that indicates the end of the data stream, DOCE (pin 7) is lowered to ensure the smooth transition of the 2 byte CRC checkword to the output line $\overline{DOUT}$ (pin 11).

DOCE must be maintained low for a minimum of 2 byte times. After the CRC word is generated, $\overline{DOUT}$ will produce a string of zeros (i.e., held high). This portion of the circuitry is dormant in the read mode.

After proper initialization, input data is entered on $\overline{DIN}$ (pin 1) along with the 2 byte CRC word for the read mode of operation. At the end of the data stream, if no errors were detected the CRCOK (pin 13) is set high. Accordingly the complimentary output (pin 16) is set low. These output states will be maintained as long as $\overline{DIN}$ is held high and $\overline{CRCIZ}$ (pin 8) is not strobed. If the CRCOK lines do not become active, an error has been detected and a re-try is in order. If successive re-tries fail, an error flag may be set to determine a further course of action as desired by the user.

WCLK is divided by 16 to produce TIMCLK which may be used as a buffered step clock for SA1000 compatible drives.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°c to 50°c
Voltage on any pin with respect to V_{SS} . . . −0.2V to +7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE
PLASTIC . . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

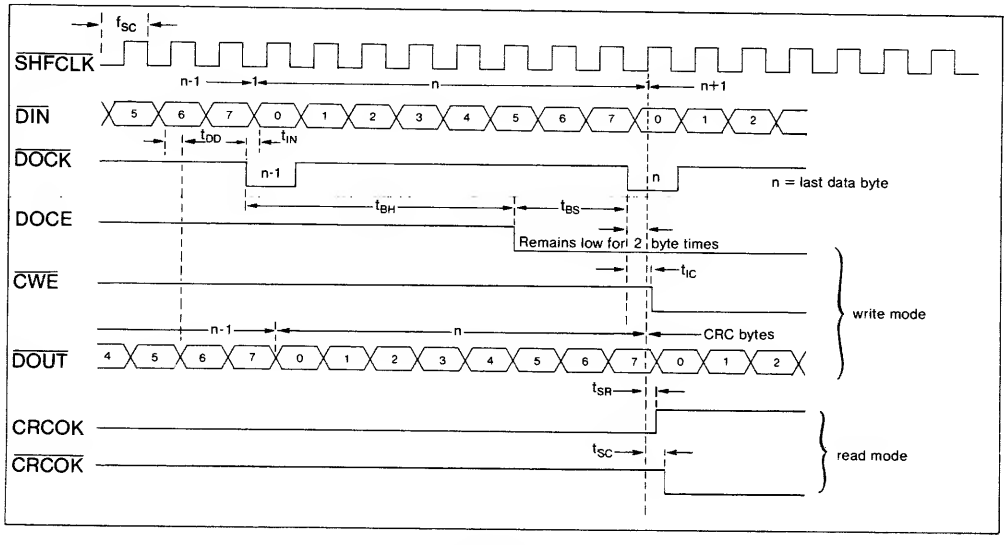
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0° to 50°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

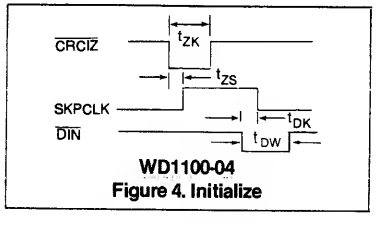
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{WT}	↑WCLK to ↓TIMCLK			95	nsec	
t_{WR}	↑WCLK to ↑TIMCLK			85	nsec	
t_{ZS}	↓$\overline{CRCIZ}$ to ↑SKPCLK			120	nsec	
t_{ZK}	$\overline{CRCIZ}$ pulse width	90			nsec	
t_{BS}	DOCE set up time w.r.t. ↓$\overline{DOCK}$	20			nsec	
t_{BH}	DOCE hold time w.r.t. ↓$\overline{DOCK}$	40			nsec	
t_{DD}	$\overline{DIN}$ to $\overline{DOUT}$ delay			105	nsec	CWE set high

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DK}	↓$\overline{DIN}$ to ↓SKPCLK			120	nsec	
t_{DW}	$\overline{DIN}$ P.W. to reset SKPCLK	50			nsec	
t_{IC}	↓$\overline{DOCK}$ to ↓$\overline{CWE}$			120	nsec	
t_{BC}	↓$\overline{DOCK}$ to ↑$\overline{CWE}$			120	nsec	
f_{SC}	$\overline{SHFCLK}$ frequency			5.25	MHZ	
t_{SR}	↑$\overline{SHFCLK}$ to ↑CRCOK			85	nsec	
t_{SC}	↑$\overline{SHFCLK}$ to ↓$\overline{CRCOK}$			90	nsec	
t_{IN}	↓$\overline{DOCK}$ to ↓$\overline{DIN}$			90	nsec	

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-04
Figure 3. Write Mode



WD1100-04
Figure 4. Initialize

See page 481 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-05 Parallel/Serial Converter

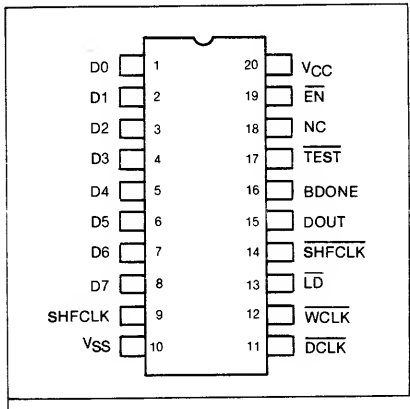
DESCRIPTION

The WD 1100-05 Parallel/Serial Converter allows the user to convert a byte of data to a serial stream when writing to a disk or any serial device. Parallel data is entered via the D0-D7 lines on the rising edge of $\overline{DCLK}$. A synchronous BYTE counter is used to signify that 8 bits of data have been shifted out and that the 8 bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.

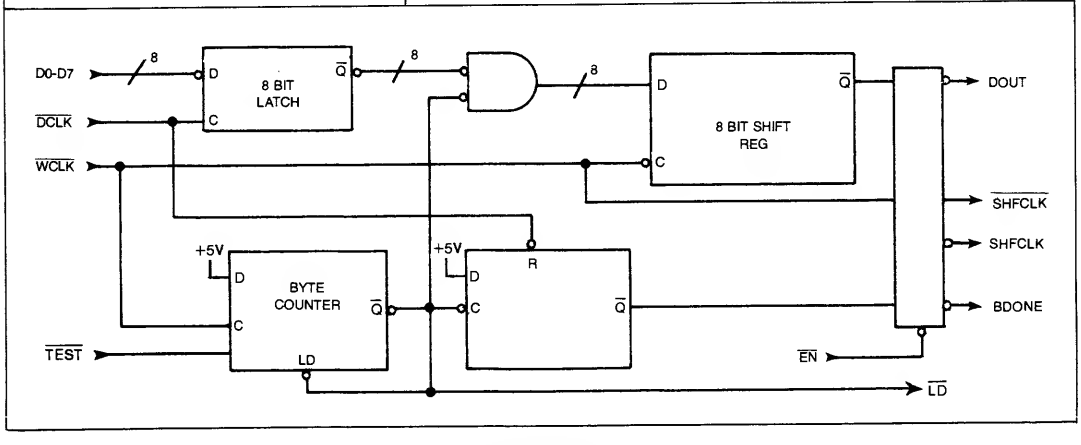
The WD1100-05 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5 M BITS/SEC SHIFT RATE
- TRI-STATE OUTPUT CONTROL
- PARALLEL IN/SERIAL OUT
- 20 PIN DIP PACKAGE



WD1100-05
Figure 1. Pin Connections



WD1100-05
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1-8	D0-D7	DATA 0-DATA 7	8 bit parallel data inputs (bit 7 = MSB).
9	SHFCLK	SHIFT CLOCK	Inverted copy of $\overline{\text{WCLK}}$ (pin 12) which is active when ENABLE (pin 19) is at a logic 0.
10	V_{SS}	GROUND	GROUND.
11	$\overline{\text{DCLK}}$	$\overline{\text{DATA CLOCK}}$	Active low input signal resets the BDONE (pin 16) latch. The low-to-high (trailing edge) clocks the input data into the internal 8 bit latch.
12	$\overline{\text{WCLK}}$	$\overline{\text{WRITE CLOCK}}$	The high-to-low (↓) edge of this clock signal is used to shift the data out serially. The low-to-high (↑) edge is used to update the internal byte counter (module 8).
13	$\overline{\text{LD}}$	$\overline{\text{LOAD}}$	This active low signal indicates that the Byte Counter is being preset to 1. Normally left open by the user.
14	$\overline{\text{SHFCLK}}$	$\overline{\text{SHIFT CLOCK}}$	Delayed copy of $\overline{\text{WCLK}}$ (pin 12) which is active when EN (pin 19) is at a logic 0.
15	DOUT	DATA OUT	Serial data output enabled by EN (pin 19).
16	BDONE	BYTE DONE	This output signal is forced to a logic 1 whenever 8 bits of data have been shifted out. BDONE remains in this state unless reset by the loading of another byte of data.
17	$\overline{\text{TEST}}$	$\overline{\text{TEST INPUT}}$	This pin must be left open by the user.
18	NC	No Connection	
19	$\overline{\text{EN}}$	$\overline{\text{ENABLE}}$	This active low signal enables DOUT, $\overline{\text{SHFCLK}}$, SHFCLK, and BDONE outputs. When high, these output signals are in a high impedance state.
20	V_{CC}	V_{CC}	+5 ± 10% power supply input.

DEVICE DESCRIPTION

Prior to loading the WD1100-05, it is recommended that 00H (or FF) be loaded into the input buffers to ensure that DOUT is at a fixed level. $\overline{\text{EN}}$ (pin 19) is set to a logic 0 to enable the device outputs.

Data is entered on the D0-D7 input lines and is strobed into the data latches on the rising edge of $\overline{\text{DCLK}}$ (pin 11). $\overline{\text{DCLK}}$ also resets BDONE (pin 16). The first BDONE that comes up simply means that the WD1100-05 is ready to accept another byte of data and that the previous byte entered is in the process of being shifted out. If the BDONE is serviced prior to every 8th WRITE CLOCK pulse the output data will represent a contiguous block of the bytes entered. Due to the asynchronous nature of the WD1100-05, the input data will be available in serial form at the output anywhere from 8 to 16 write clock cycles later.

Data is shifted out on the high-to-low (↓) transition of the $\overline{\text{WCLK}}$ (pin 12). The low-to-high (↑) transition of $\overline{\text{WCLK}}$ increments a byte counter which in turn sets the BDONE signal high after 8 bits of data have been shifted out. The low-to-high transition of BDONE also causes the loading of the data buffer into the shift register. The data buffer is now ready to be reloaded with the next byte.

The loading of the next byte automatically clears the BDONE signal. The entire process as outlined above is repeated. BDONE always needs to be serviced within 8 $\overline{\text{WCLK}}$ cycles unless the next byte to be transmitted is the same as the previous byte.

Four signals, BDONE, DOUT, $\overline{\text{SHFCLK}}$, and SHFCLK, can be placed in a high impedance state by setting $\overline{\text{EN}}$ (pin 19) to a logic 1. Likewise, $\overline{\text{EN}}$ must be at a logic 0 in order for these signals to drive any external device.

The $\overline{\text{TEST}}$ pin is internally OR'ed with the counter output to produce the $\overline{\text{LD}}$ (pin 13) signal. This is used to inhibit the bit counter by external means for test purposes. It is recommended that $\overline{\text{TEST}}$ be left open by the user. An internal pullup register is tied to this pin to satisfy the appropriate logic level required for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... 0°C to 50°C
Voltage on any pin with respect to V_{SS} ... −0.2V to +7.0V
Power Dissipation ..... 1 Watt
STORAGE TEMPERATURE
PLASTIC ..... −55°C to +125°C
CERAMICS ..... −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions s 3 .ed in the DC electrical characteristics.

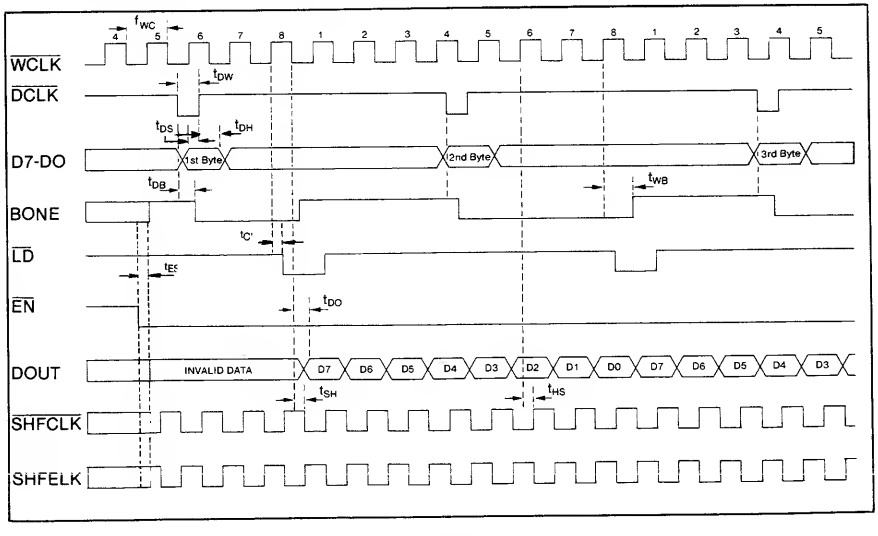
DC Electrical Characteristics: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{OH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC Electrical Characteristics: T_A = 0°C to 50°C; V_{CC} = +5 ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK frequency			5.25	MHZ	
t_{DW}	DCLK pulse width	50			nsec	
t_{DS}	Data set-up w.r.t. ↑ DCLK	30			nsec	
t_{DH}	Data hold time w.r.t. ↑ DCLK	30			nsec	
t_{DB}	↓ DCLK to ↓ BDONE			130	nsec	EN = 0
t_{DO}	↓ WCLK to DOUT			130	nsec	EN = 0
t_{SH}	↓ WCLK to ↓ SHFCLK			75	nsec	EN = 0
t_{HS}	↑ WCLK to ↑ SHFCLK			70	nsec	EN = 0
t_{WB}	↑ WCLK to ↑ BDONE	75		180	nsec	
t_{ES}	↓ $\overline{EN}$ to BDONE, DOUT SHFCLK ACTIVE			25	nsec	
t_{CL}	↑ $\overline{WCLK}$ to ↓ $\overline{LD}$			50	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-05

Figure 3. Functional Timing Diagram

See page 481 for ordering information.

Printed in U.S.A.

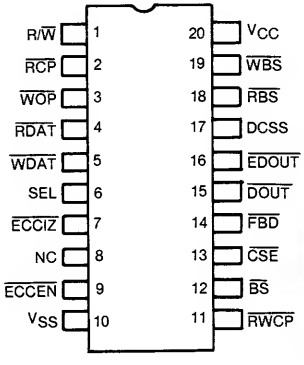
Western Digital
WD1100-06 ECC/CRC Logic

DESCRIPTION

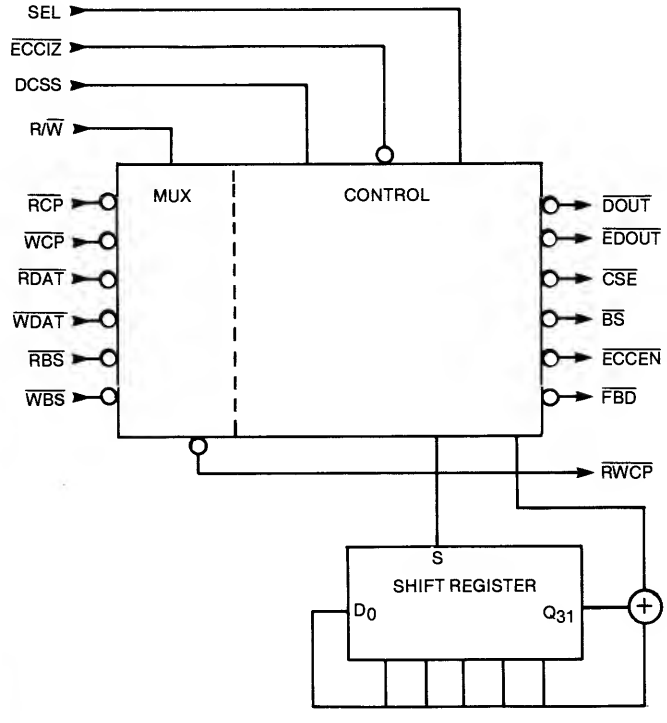
The WD1100-06 ECC/CRC logic chip gives the user of the WD1100 series of chips easy ECC or CRC implementation. With proper software, it will provide single burst correction up to 8 bits and double burst detection. The computer selected polynomial has been optimized for Winchester 5¼" and 8" drives with sector sizes up to 512 bytes.

FEATURES

- 32 bit computer selected polynomial
- Single burst correction up to 8 bits
- Multiple burst detection
- Programmable correction/detection span
- CRC or ECC software selectable
- Data transfer rates to 5.25 Mbits/sec
- Serial check/syndrome bit processing
- 128, 256, 512 byte sector sizes
- Single +5V supply
- TTL, MOS compatible
- 20 pin DIP package



WD1100-06 Figure 1.
PIN CONNECTIONS



WD1100-06 Figure 2.
BLOCK DIAGRAM

WD1100-06 ECC/CRC DEVICE PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ/WRITE	R/$\overline{W}$	Input line used to select the data, clock and CRC/ECC strobe during read/write operations. When low input signals $\overline{WDAT}$, $\overline{WCP}$, and $\overline{WBS}$ are selected. When high input signals $\overline{RDAT}$, $\overline{RCP}$, and $\overline{RBS}$ are selected.
2	$\overline{\text{READ CLOCK PULSE}}$	$\overline{RCP}$	Input pulse used by the internal shift registers to compute the 4 syndrome bytes.
3	$\overline{\text{WRITE CLOCK PULSE}}$	$\overline{WCP}$	Input pulse used by the internal shift registers to compute the 4 check bytes.
4	$\overline{\text{READ DATA}}$	$\overline{RDAT}$	Serial data input during a read operation.
5	$\overline{\text{WRITE DATA}}$	$\overline{WDAT}$	Serial data input during a write operation.
6	SELECT	SEL	This input is used to select either the CRC or the ECC polynomial for error detection/correction. SEL = 0 ECC polynomial selected. SEL = 1 CRC polynomial selected.
7	$\overline{\text{ECC INITIALIZE}}$	$\overline{ECCIZ}$	Input used to preset all the internal shift registers. Output lines $\overline{FBD}$, $\overline{EDOUT}$, $\overline{DOUT}$, and $\overline{CSE}$ will be in their inactive high states. The first low going edge of either $\overline{RDAT}$ or $\overline{WDAT}$ signals the activation of all internal circuitry.
8	NO CONNECTION	N/C	No connection.
9	$\overline{\text{ECC ENABLE}}$	$\overline{ECCEN}$	When low, the ECC/CRC process is enabled. When high, this output signal indicates that the process is disabled.
10	GROUND	V_{SS}	Ground
11	$\overline{\text{READ/WRITE CLOCK PULSE}}$	$\overline{RWCP}$	Output clock pulse during read or write operations. The input clock pulses $\overline{RCP}$ and $\overline{WCP}$ are multiplexed on this output line for use by any support logic.
12	$\overline{\text{BYTE SYNC}}$	$\overline{BS}$	The input signals $\overline{RBS}$ and $\overline{WBS}$ are gated with the appropriate clocks and multiplexed as an output on the byte sync line. Normally not used by the user.
13	$\overline{\text{CLOCK SELECT ENABLE}}$	$\overline{CSE}$	When high, this output indicates that the device is in the process of computing the check/syndrome bytes and that $\overline{EDOUT}$ and $\overline{DOUT}$ lines contain data information. When low, the device puts CRC or ECC check/syndrome bits on the output data lines.
14	$\overline{\text{FEEDBACK}}$	$\overline{FBD}$	The feedback line to the shift registers is brought out as an output line for test purposes. Normally left open by the user.
15	$\overline{\text{DATA OUTPUT}}$	$\overline{DOUT}$	Output data line carries data or CRC/ECC information depending upon the state of DCSS.
16	$\overline{\text{EARLY DATA OUTPUT}}$	$\overline{EDOUT}$	Unlatched output data line available 1 clock period earlier than $\overline{DOUT}$.

WD1100-06 ECC/CRC PIN DESCRIPTION (CONTINUED)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
17	DATA/CHECK SYNDROME SELECT	DCSS	Data or check/syndrome select input line. When high, data is output on the data lines; when low, CRC or check syndrome bits are output depending upon which polynomial is selected. DCSS goes low sometime between the last and the next to the last data byte transferred to/from the disk provided all set-up and hold-times have been met. DCSS must stay low for at least 2 byte times when the CRC polynomial selected and it must stay low for at least 4 byte times if the ECC polynomial is selected.
18	$\overline{\text{READ BYTE}}$	$\overline{\text{RBS}}$	Input used to latch the state of DCSS during the read mode.
19	$\overline{\text{WRITE BYTE}}$	$\overline{\text{WBS}}$	Input used to latch the state of DCSS during the write mode.
20	+5V	V_{CC}	+5V ±10%

DEVICE DESCRIPTION

To ensure correct operation of the WD1100-06 device, the $\overline{\text{ECCIZ}}$ line is strobed to preset the polynomial generator shift register, and reset the Data/Check-Syndrome select flip-flop. The 32 bit shift register string is preset to avoid all zero check bytes. The DCSS line is held high and appropriate signals are then applied to the rest of the inputs. Since most disk media use an Address mark of A1 (or M.S.B. set), advantage is taken of this feature to start off the ECC/CRC calculation on the data/ID fields automatically. The first active low going edge on the input data lines releases the internal SET Flip-Flop. The $\overline{\text{ECCEN}}$ output line is set low indicating that the internal circuitry is ready to begin the computation of the ECC/CRC bytes. Immediately following the Address mark, data is supplied in a serial fashion.

Sometime before the last byte of data and after the next to the last byte of data is transferred through this device, the DCSS line is set low. Since data is generally serialized/deserialized before/after processing by the WD1100-06 device, the byte-sync pulses can be easily obtained from those devices marking the byte boundaries. The byte-sync pulses are internally ANDED with the $\overline{\text{RWCP}}$ line to ensure the smooth transition of check/syndrome bytes on the $\overline{\text{DOUT}}$ output line only after the last bit of data has been entered into the device. A one bit time delay through a D Flip-Flop has been added on the $\overline{\text{DOUT}}$ line to deglitch this output line.

During a WRITE operation, the input data stream is divided by the polynomial $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^2 + 1$ and the 32 bit remainder obtained is used as the 4 check syndrome bytes. If the syndrome is zero, no errors occurred. Otherwise, the non-zero syndrome is used by a software algorithm to compute the displacement and the error vector within the bad sector. To protect the integrity of the ID field only a CRC check should be performed over this field. No attempt ought to be made to correct data in the ID field. The CRC polynomial implemented is the standard CCITT ($X^{16} + X^{12} + X^5 + 1$.) Although either polynomial may be used for both fields, the use of the CRC polynomial for the ID fields is recommended since it only requires 2 bytes instead of 4.

POLYNOMIAL SELECTION

For disk media, polynomial selection has a significant influence on data accuracy. Fire code polynomials have been widely used on OEM disk controllers, but provide less accuracy than properly selected computer generated codes.

For fixed, guaranteed correction and detection spans, data accuracy may be highly dependent on polynomial selection. Some polynomials, fire codes for example, are particularly susceptible to miscorrection on common disk type errors, while others, computer generated polynomials for example, can be selected to be less susceptible. Computer generated codes do not have the pattern sensitivity of the fire code and the miscorrection patterns are more random in nature.

More than 20,000 computer generated random polynomials of degree 32, each with 8 feedback terms, were evaluated in order to find the polynomial described in this specification.

SELECTING THE CORRECTION SPAN

The code described in this document can be used to correct up to 8 bits.

Any correction span from 1 to 8 may be selected. However, for best data accuracy, the lowest correction span should be used that meets the correction

requirements for the disk drives supported.

For most Winchester media, a 5 bit correction span is adequate.

The correction span may have to be longer if the drive uses a read/write modulation method that maps a single media bit in error into several decoded bits in error. Examples of read/write modulation methods of this type would be GCR and 2,7 code.

PROPERTIES OF THE POLYNOMIAL

The following polynomial was computer selected for insensitivity to short double bursts, good detection span and 8 feedback terms.

Forward polynomial is:
$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 0$

Reciprocal polynomial is:
$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + x^{13} + X^6 + X^4 + X^0$

Properties*

1. Maximum record length (r) = 526x8 bits (including check bits)
2. Maximum correction span (b) = 8 bits
3. Degree of polynomial (m) = 32
4. Single burst detection span without correction = 32 bits. (Detection span when the code is used for detection only)
5. Single burst detection span with correction (d) — (Detection span when the code is used for correction)
   - = 19 bits for b = 5 and r = 526x8
   - = 14 bits for b = 8 and r = 526x8
   - = 20 bits for b = 5 and r = 270x8
   - = 14 bits for b = 8 and r + 270x8
6. Double burst detection span without correction — (Doule burst detection span when code is used for correction)
   - = 3 bits for b = 5 and r = 526x8
   - = 2 bits for b = 8 and r = 526x8
   - = 4 bits for b = 5 and r = 270x8
   - = 2 bits for b = 8 and r = 270x8
7. Non-detection probability = 2.3 E-10.
8. Miscorrection probability—
   - = 1.57 E-5 for b = 5 and r = 526x8
   - = 1.25 E-4 for b = 8 and r = 526x8
   - = 8.00 E-6 for b = 5 and r = 270x8
   - = 6.40 E-5 for b = 8 and r = 270x8

NOTE:*
You should not use this polynomial for a record length or correction span beyond the maximum specified above.

SOFTWARE REQUIREMENTS

The software algorithm, developed by the user, uses the syndrome to detect an error, generate a correction pattern and a displacement vector or to determine if uncorrectable. In the correction algorithm, a simulated shift register is used to implement the reciprocal polynomial. The simulated shift register is loaded with the syndrome and shifted until a correctable pattern is found or the error is determined to be uncorrectable. Both forward and reverse displacements are computed.

Either the serial or the parallel algorithm may be implemented by the user. In almost all cases the serial software algorithm is the most applicable. Additionally, 1K of table space is required if the parallel software algorithm is selected. It is assumed that the highest order bit of a byte is serialized and deserialized first.

CORRECTION TIME PERFORMANCE

All real time operations are performed with error correction hardware. The software algorithms used get involved only after an error has been detected.

The following correction times are for a serial type algorithm such as that used on the WD1001:

a) Standard microprocessor = 30 to 60 milliseconds
b) Bit slice = 6 to 12 milliseconds
c) 8X300 (used on WD1001) = 15 to 30 milliseconds

DATA ACCURACY

ERP (Error Recovery Procedure) strategies have a significant influence on data accuracy. An ERP strategy requires data to be re-read before applying correction and results in much better data accuracy. The WD1001 employs such a strategy. This strategy reduces the possibility of passing undetected erroneous data by rereading until the error goes away, or until there has been a consistant error syndrome over two previous rereads.

Another technique that can be used to give data a higher probability of recovery is write check: read back after write. Since write check affects performance, it should be optional. Alternate sector assignment and defect skipping are some of the other techniques that may be implemented by the user if so desired.

SELF-CHECKING WITH MICROCODE

Periodic microcode and/or software checking is another approach that can be used to limit the amount of undetected erroneous data transferred in case of an ECC circuit failure. Microcode or software diagnostics could be run on subsystem power up and during idle times. These diagnostics would force ECC errors and check for the proper syndrome and proper decoding of the syndrome by the correction routine of the operational microcode.

To do this, simply use a long bit in the READ and WRITE commands to the disk. This bit can then be used to suppress the transfer of check/syndrome bytes on the output data line by letting the DCSS line stay high during ECC TIME. The complete procedure is summarized below.

1. WRITE: Pass all data to the disk and generate 4 check bytes at the end of the data field.
2. READLONG: Do not generate the syndrome, instead copy the 4 check bytes as data and pass them unaltered to the host. Now the host may induce errors anywhere in the data stream as long as the induced error does not exceed the correction span of the polynomial generator.
3. WRITELONG: Write the data and check bytes supplied by the host to the disk. Prevent WD1100-06 from generating check bits by not asserting DCSS during transfer. No check bytes will be recorded.
4. READ: Read data and generate the syndrome in a normal manner. The software algorithm can now be invoked to correct the induced error.

To aid in detection of certain hardware failures, it is desirable to have non-zero check bytes for an all zeros record. This feature has been incorporated into the circuit defined in this specification.

SPECIFICATIONS

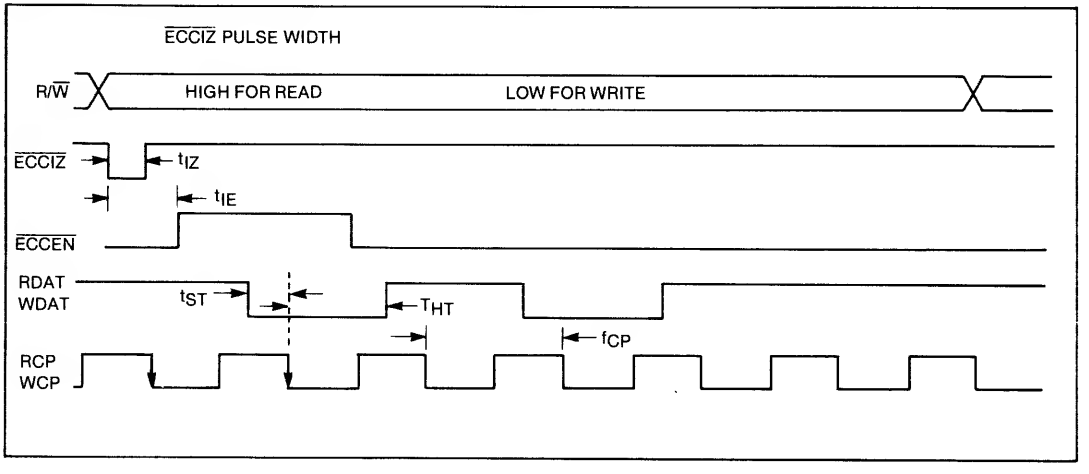
ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias ..... 0°C to 50°C
Voltage on any pin with
respect to V_{SS} ..... −0.2V to +7.0V
Power dissipation ..... 1 Watt
Storage Temperature
Plastic ..... −55°C to +125°C
Ceramic ..... −55°C to +150°C

NOTE:
Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		75	150	mA	All outputs open



AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS}

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{CP}	Clock Frequency			5.25	MHZ	
t_{IZ}	$\overline{ECCIZ}$ Pulse Width	50			nSec	
t_{IE}	$\overline{ECCIZ}$ ↓ to $\overline{ECCEN}$ ↑			100	nSec	
t_{ST}	R/WDAT Setup Time	50		1 Clock Period	nSec	
t_{HT}	R/WDAT Hold Time	0			nSec	

See page 481 for ordering information.

Western Digital
WD1100-07 Host Interface Logic

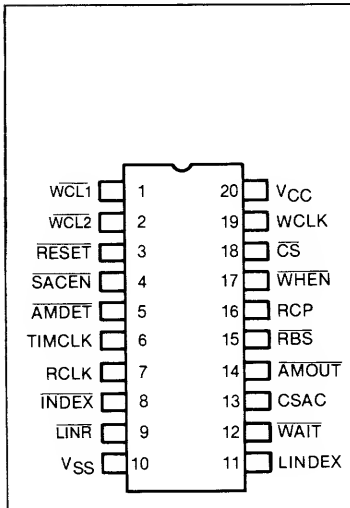
DESCRIPTION

The WD1100-07 Host Interface Logic chip simplifies the design of a Winchester Hard Disk Controller using the WD1100 chip series. It does this by performing logic functions that would otherwise require considerable discrete logic. Additionally, there are signals provided for ECC implementation.

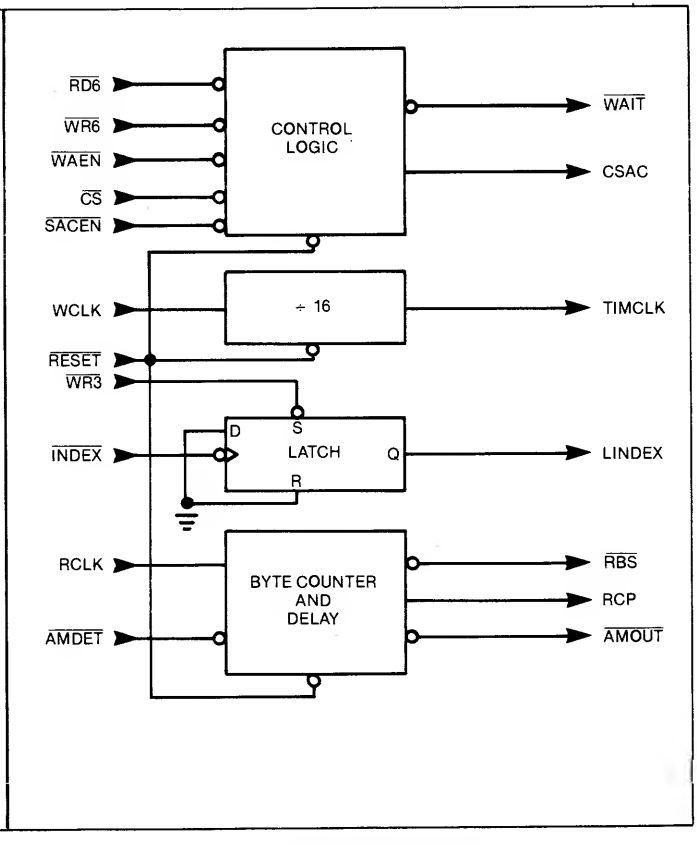
The WD1100-07 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic Dual-in-Line package.

FEATURES

- SINGLE +5V SUPPLY
- WAIT SIGNAL GENERATION
- TIMING CLOCK GENERATION
- INDEX PROPAGATION
- CARD ACCESS CONTROL
- COMPLIMENTS ECC ARCHITECTURE
- 20 PIN DIP PACKAGE



WD1100-07 Figure 1.
PIN CONNECTIONS



WD1100-07 Figure 2.
BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	WAIT CLEAR 1	$\overline{WCL1}$	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
2	WAIT CLEAR 2	$\overline{WCL2}$	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
3	RESET	$\overline{RESET}$	An input used to set TIMCLK & reset $\overline{WAIT}$, $\overline{AMOUT}$ and $\overline{RBS}$.
4	SELECT ADDRESS ENABLE	$\overline{SACEN}$	This is an input signal that is used to enable card select for host access.
5	ADDRESS MARK DETECT	$\overline{AMDET}$	An input that must go active when a DATA = A1(HEX) or clock = 0A(HEX) pattern is detected in the data stream
6	TIMING CLOCK	TIMCLK	An output used to provide reference timing signals to SA100 type drives
7	READ CLOCK	RCLK	This input, the same as used to clock in data and clocks to the AM detector, is used to produce $\overline{AMOUT}$.
8	INDEX PULSE	$\overline{INDEX}$	This input is provided by the drive once each revolution of the disk
9	LINDEX RESET	$\overline{LINR}$	An input used to reset LINDEX.
10	GROUND	V_{SS}	Ground
11	LATCHED INDEX	LINDEX	An output that is $\overline{INDEX}$ delayed by one clock time.
12	WAIT	$\overline{WAIT}$	This output goes true when controller is internally accessing data or has not accepted data from the host during a WRITE.
13	CARD SELECT ADDRESS	CSAC	An output that is the result of $\overline{CS}$ qualified with $\overline{SACEN}$.
14	ADDRESS MARK DELAYED OUTPUT	$\overline{AMOUT}$	This output is a delayed version of $\overline{AMDET}$.
15	READ BYTE STROBE	$\overline{RBS}$	This output strobes once for each byte of READ data. Initialized by $\overline{AMDET}$.
16	READ CLOCK PULSE	RCP	This output is delayed from RCLK through propagation. Not normally used.
17	WAIT ENABLE	$\overline{WAEN}$	An input that is used to enable the internal WAIT circuitry.
18	CARD SELECT	$\overline{CS}$	An input from host that selects controller.
19	WRITE CLOCK	WCLK	This input is used to produce TIMCLK on low to high transitions.
20	+5VDC	V_{CC}	+5V ± 10%

DEVICE DESCRIPTION

Upon power up or reset, $\overline{WAIT}$, $\overline{AMOUT}$, and $\overline{RBS}$ are reset and TIMCLK is set. This is the only interactive signal between the four sections of the chip. Each section will be described separately.

Control Logic

This section provides $\overline{WAIT}$ (pin 12) and CSAC (pin 13). $\overline{WAIT}$ is set in its active low state when $\overline{WAEN}$ (pin 17) is active low by the falling edge of $\overline{CS}$ (pin 18). $\overline{WAIT}$ is reset by the falling edge of either $\overline{WCL1}$ or $\overline{WCL2}$ depending on whether in a read or write mode. CSAC (pin 13) is enabled by setting $\overline{SACEN}$ (pin 4) low after $\overline{WAIT}$ has been enabled. CSAC is reset by $\overline{WCL1}$ or $\overline{WCL2}$.

Timing Clock

TIMCLK (pin 6) is a divided by sixteen version of WCLK (pin 19). It is used with SA1000 type drives.

Index Pulse

Lindex (pin 11) is a delayed version of $\overline{INDEX}$ (pin 8). It remains high until reset by $\overline{LINR}$ (pin 9).

Read Byte Sync

$\overline{RBS}$ (pin 15) will go true on the eighth negative going transition of RCLK (pin 7) after $\overline{AMDET}$ (pin 5) goes true. $\overline{RBS}$ will remain true for one clock cycle.

Read Clock Pulse

RCP (pin 16) is a delayed version of RCLK and is normally left open by the user.

Address Mark Delayed Output

$\overline{AMOUT}$ (pin 14) is the same as $\overline{AMDET}$ delayed by two clock times.

These circuits were developed to work with the other chips in the WD1100 series. They are used on the WD1001 the timing relationships must be observed.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... 0°C to 50°C
Voltage on any pin with
respect to V_{SS} ..... −0.2V to +7.0V
Power Dissipation ..... 1 Watt
Storage Temperature Plastic −55°C to +125°C
Ceramic −55°C to +150°C

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

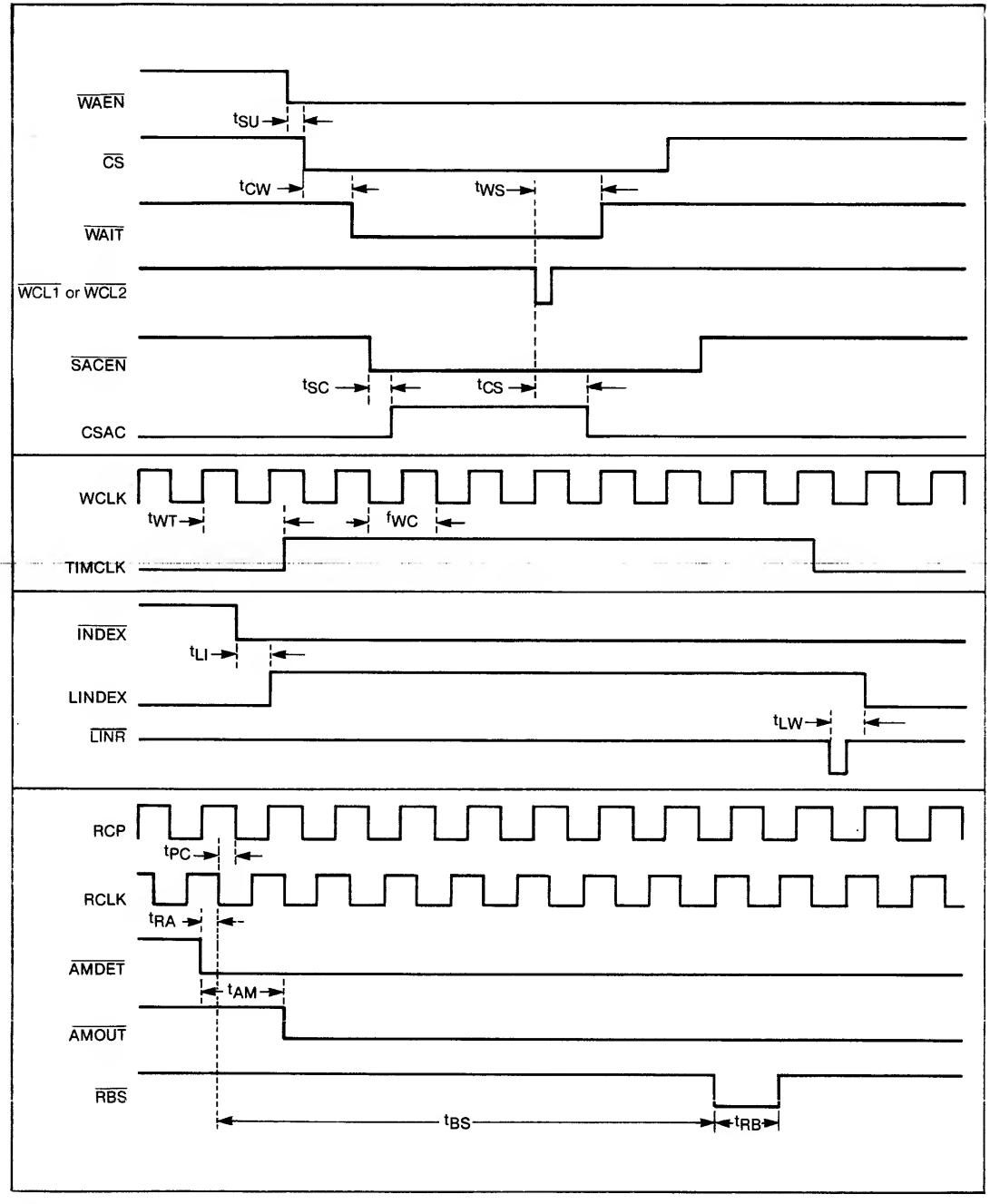
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK FREQUENCY			5.25	MHZ	
t_{CW}	$\overline{CS}$↓ to $\overline{WAIT}$↓		50	160	nSec	
t_{WS}	$\overline{WCL1}$↓ or $\overline{WCL2}$↓ to $\overline{WAIT}$↑		170	195	nSec	
t_{SU}	$\overline{WAEN}$ Setup Time	50			nSec	
t_{SC}	$\overline{SACEN}$↓ to CSAC↑		5	70	nSec	$\overline{WAIT}$ TRUE
t_{CS}	$\overline{WCL1}$↓ or $\overline{WCL2}$↓ to CSAC↓		45	155	nSec	$\overline{WAIT}$ TRUE
t_{WT}	WCLK↑ to TIMCLK↑			250	nSec	
t_{LI}	$\overline{INDEX}$↓ to LINDEX↑		50	100	nSec	
t_{LW}	$\overline{LINR}$↓ to LINDEX↓		30	100	nSec	
t_{PC}	RCLK↓ to RCP↓		30	75	nSec	
t_{RA}	$\overline{AMDET}$ Setup Time	30	50		nSec	
t_{AM}	$\overline{AMDET}$↓ to $\overline{AMOUT}$↓		2 CLOCK CYCLES	2 CLOCK CYCLES +45	nSec	
t_{BS}	RCLK↓ to $\overline{RBS}$↓		8 CLOCK CYCLES	8 CLOCK CYCLES +165	nSec	
t_{RB}	$\overline{RBS}$ Period		1 CLOCK CYCLE			

[1] NOTE: Typical Values are for T_A = 25°C and V_{CC} = +5V



See page 481 for ordering information.

Western Digital
WD1100-09 Data Separator Support Logic

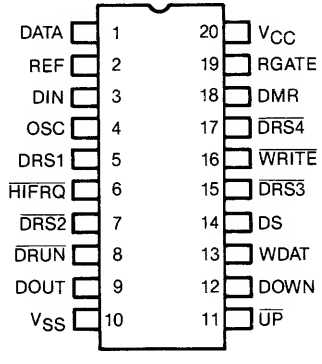
GENERAL DESCRIPTION

The WD1100-09 Data Separator Support Logic, when used with the other chips in the WD1100 series, greatly reduces the external discrete logic required to design a Winchester hard disk data separator. The chip provides the pump signals to an external error amplifier, control signals to an internal bus and a special drive selection signal also to an internal bus.

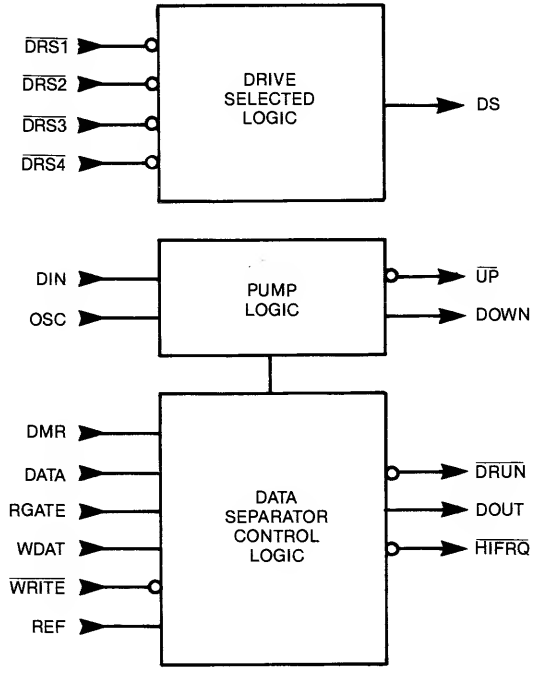
The WD1100-09 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic package.

FEATURES

- SINGLE +5V SUPPLY
- DRUN GENERATION
- DATA SEPARATION CONTROL SIGNALS
- 20 PIN DIP PACKAGE



WD1100-09 Figure 1.
PIN CONNECTIONS



WD1100-09 Figure 2.
BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ DATA	DATA	Input that is used in $\overline{\text{DRUN}}$ generation.
2	REFERENCE	REF	An input that is 2 times the data rate that keeps the VCO on center frequency during non-read times.
3	DELAYED DATA IN	DIN	This input is a delayed version of DOUT. An external delay line is used. The signals are compared to provide pumps.
4	OSCILLATOR	OSC	An input from the external VCO that is used in pump development
5, 7, 15, 17	$\overline{\text{DRIVE SELECT}}$ 1- $\overline{\text{DRIVE SELECT}}$ 4	$\overline{\text{DRS1}}$- $\overline{\text{DRS4}}$	Input signals indicating which drive has been selected.
6	$\overline{\text{HIGH FREQUENCY}}$	$\overline{\text{HIFRQ}}$	Output to controller microprocessor that indicates 16 ones or zeros have been entered on the DATA line.
8	$\overline{\text{DATA RUNNING}}$	$\overline{\text{DRUN}}$	Output that indicates to the controller microprocessor the completion of 16 ones or zeros on the data line. Used to switch from REF to DATA via firmware.
9	DATA OUT	DOUT	Output data line. Can be REF or DATA or WDATA depending on the condition of $\overline{\text{WRITE}}$, $\overline{\text{DMR}}$ and RGATE.
10	GROUND	V_{SS}	Ground
11	$\overline{\text{UP PUMP}}$	$\overline{\text{UP}}$	An output that indicates REF is leading DATA. Goes to error amp. Open collector.
12	DOWN PUMP	DOWN	An output that indicates DATA is leading REF. Goes to error amp. Open collector.
13	WRITE DATA	WDATA	MFM Write data input. Output appears at DOUT.
14	DRIVE SELECTED	DS	An output that indicates that one of four drives have been selected.
16	$\overline{\text{WRITE MODE}}$	$\overline{\text{WRITE}}$	This input is active during a write operation and enables WDAT.
18	DATA MASTER RESET	DMR	This input is used to provide time-out for $\overline{\text{DRUN}}$ and $\overline{\text{HIFRQ}}$ in the event that 16 ones or zeros are not present.
19	READ GATE	RGATE	This input, usually provided by the controller microprocessor, places chip in read mode.
20	+5VDC	V_{CC}	+5VDC ± 10%

DEVICE DESCRIPTION

The WD1100-09 is divided into three sections. Each section will be described separately.

Drive Select Logic

DS (pin 14) will go active high if any input $\overline{\text{DSR1}}$ through $\overline{\text{DRS4}}$ (pins 5, 7, 15, 17) are active low.

Pump Logic

Internal logic causes the $\overline{\text{UP}}$ (pin 11) and the DOWN (pin 12) to be set, initially to their inactive states. DIN (pin 3) is the delayed data developed by passing DOUT through a delay line. OSC (pin 4) is the output of the data separator VCO. Whichever reaches the pump logic first will determine whether UP PUMP or DOWN PUMP is produced. These signals are then sent to an external error amplifier and used for VCO correction. During a write, the DIN must be locked to a crystal oscillator clock and will hold the VCO on frequency.

Data Separator Control Logic

Read Mode

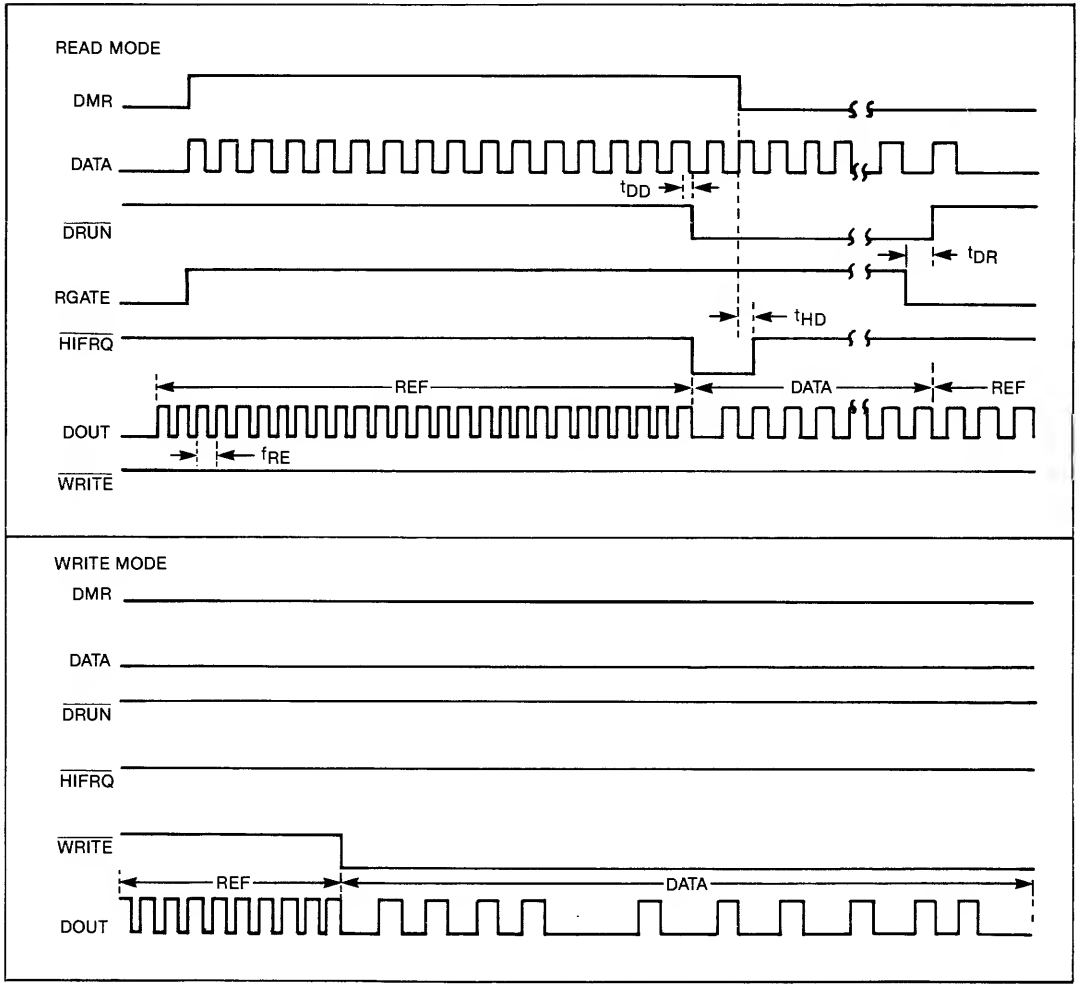
In order to prevent the external VCO from locking onto a harmonic of its operating frequency, REF (pin 2) is provided with a signal twice the data rate that is crystal controlled. With $\overline{\text{WRITE}}$ (pin 6) and RGATE (pin 19) inactive, this signal will appear at DOUT (pin 9). This signal is applied to the pump logic (see above).

The switching function is initiated immediately after RGATE goes true. DMR (pin 18) will be set active as a result of high frequency pulses applied to an external one shot whose pulse width is such that its output is a single stretched pulse. The high frequency pulses are applied to the DATA (pin 1) line and after 16 consecutive pulses, $\overline{\text{DRUN}}$ (pin 8) and $\overline{\text{HIFRQ}}$ (pin 6)

go true. At this point REF is switched out and the DATA stream is switched in and appears at DOUT. $\overline{\text{DRUN}}$ is reset when RGATE goes inactive and $\overline{\text{HIFRQ}}$ goes inactive when DMR goes inactive.

Write Mode

When $\overline{\text{WRITE}}$ (pin 16) goes active, REF is switched out and WDAT (pin 13) will appear at DOUT. Since WDAT is a crystal controlled signal (usually the MFM write data); the VCO is held locked and will not drift (see pump logic above).



AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DD}	DATA↓ to $\overline{\text{DRUN}}$↓			170	nSec	
t_{DR}	RGATE↓ to $\overline{\text{DRUN}}$↑			90	nSec	
t_{HD}	DMR↓ to $\overline{\text{HIFRQ}}$↑			90	nSec	
f_{RE}	REF frequency		2 TIMES DATA RATE	10	MHz	

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin with
respect to V_{SS} . . . . . −0.2V to +7.0V
Power Dissipation . . . . . 1 Watt
Storage Temperature Plastic −55°C to +125°C
Ceramic −55°C to +150°C

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

NOTE: $\overline{UP}$ and DOWN are open collector outputs and provide 12mA I_{OL} @ .5V.

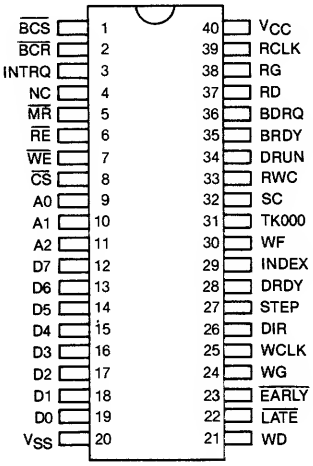
See page 481 for ordering information.

Printed in U.S.A.

WD1010-00/01 Winchester Disk Controllers

FEATURES

- ST506/SA1000 COMPATIBLE
- MULTIPLE SECTOR READ/WRITE
- UP TO 5MBITS/SEC DATA RATE
- UNLIMITED SECTOR INTERLEAVE
- AUTOMATIC FORMATTING
- CRC/ECC CAPABILITY
- AUTOMATIC RETRIES (WD1010-00 ONLY)
- VARIABLE SECTOR SIZE
- SINGLE +5V SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1010 is a MOS/LSI device which performs the functions of a Winchester Disk Controller/Formatter. It is compatible with the Seagate ST506 and the Shugart Associates SA1000 drives, as well as all other 5¼" and 8" products utilizing the same type of interface. On the host side, an 8 bit bi-directional bus accepts all commands, data, and status bytes. The Western Digital WD1000 series of board level controllers are software compatible with the WD1010.

Operating from a single 5 volt supply, the WD1010 is implemented in NMOS silicon gate technology and is available in a 40 pin dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
12-19	DATA 7 - DATA 0	D7-D0	Eight bit tristate bidirectional bus used for transfer of commands, status, and data.
6	READ ENABLE	$\overline{RE}$	Tristate bidirectional line, used as an input for reading the task register and an output when WD1010 is reading the buffer.
7	WRITE ENABLE	$\overline{WE}$	Tristate bidirectional line used as an input for writing into the task register and as an output when the WD1010 is writing to the buffer.
9-11	ADDRESS 0 - ADDRESS 2	A0-A2	These three inputs select the register to receive/transmit data on D0-D7.
8	CHIP SELECT	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
3	INTERRUPT REQUEST	INTRQ	Active high output which is set to a logic high in the completion of any command.
5	MASTER RESET	$\overline{MR}$	A logic low in this input will initialize all internal logic.
1	BUFFER CHIP SELECT	$\overline{BCS}$	Active low output used to enable reading or writing of the external sector buffer.
35	BUFFER READY	BRDY	This rising edge activated input is used to inform the controller that the sector buffer is full or empty.
2	BUFFER COUNTER RESET	$\overline{BCR}$	Active low output that is strobed by the WD1010 prior to read/write operations. This pin is strobed whenever $\overline{BCS}$ changes state.
36	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the sector buffer.
40	+5 VOLT	V_{CC}	+5V ±5% Power supply input.
20	GROUND	V_{SS}	Ground
4	NO CONNECT	NC	
21	WRITE DATA	WD	This open drain output contains the MFM clock and data pulses to be written on the disk.
25	WRITE CLOCK	WCLK	4.34 or 5.0 Mhz clock input used to derive all internal write timing.
24	WRITE GATE	WG	This output is set to a logic high before writing is to be performed on the disk.
23, 22	EARLY, LATE	$\overline{EARLY}$, $\overline{LATE}$	Precompensation open drain outputs used to delay the WD pulses externally.
37	READ DATA	RD	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
39	READ CLOCK	RCLK	A nominal square wave clock input derived from the external data recovery circuits.
38	READ GATE	RG	This output is set to a logic high when data is being inspected from the disk.
34	DATA RUN	DRUN	This input informs the WD1010 when a field of one's or zeroes have been detected.
27	STEP PULSE	STEP	This output generates a pulse for stepping the drive motor.
26	DIRECTION	DIR	This output determines the direction of the stepping motor.
28	DRIVE READY	DRDY	This input must be at a logic high in order for commands to execute.
30	WRITE FAULT	WF	An error input to the WD1010 which indicates a fault condition at the drive.

PIN DESCRIPTION (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	TRACK 000	TK000	An input to the WD1010 which indicates positioning over track 000.
29	INDEX PULSE	INDEX	A logic high on this input informs the WD1010 when the index hole has been encountered.
33	REDUCED WRITE CURRENT	RWC	This output can be programmed to reduce write current on a selected starting cylinder.
32	SEEK COMPLETE	SC	This input informs the WD1010 when head settling time has expired.

ARCHITECTURE

The WD1010 Winchester Disk Controller provides the necessary link between an 8-bit, parallel processor and a Winchester disk drive. Two versions of the WD1010 are available. The WD1010-00 has automatic retries on errors. The WD1010-01 terminates the command execution on errors. These differences are noted in the following text and flowcharts. The internal architecture of the WD1010 is shown in Figure 1. Its major functional blocks are:

PLA Controller

The PLA interprets commands and provides all control functions. It is synchronized with WCLK.

Magnitude Comparator

A 10 bit magnitude comparator is used for calculation of drive step, direction, present and desired cylinder position.

CRC Logic

Generates and checks the cyclic redundancy check characters appended to the ID and data fields. The polynomial is X16 + X12 + X5 + 1.

MFM Encode/Decode

Encodes and decodes MFM data to be written/read from the drive. The MFM encoder operates from WCLK; a clock having a frequency equivalent to the bit rate. The MFM decode operates from RCLK; a bit rate clock generated from the external data separator. RCLK and WCLK need not be synchronized.

AM Detect

The address mark detector checks the incoming data stream for a unique missing clock pattern (Data = H'A1', Clock = H'0A') used in each ID and data field.

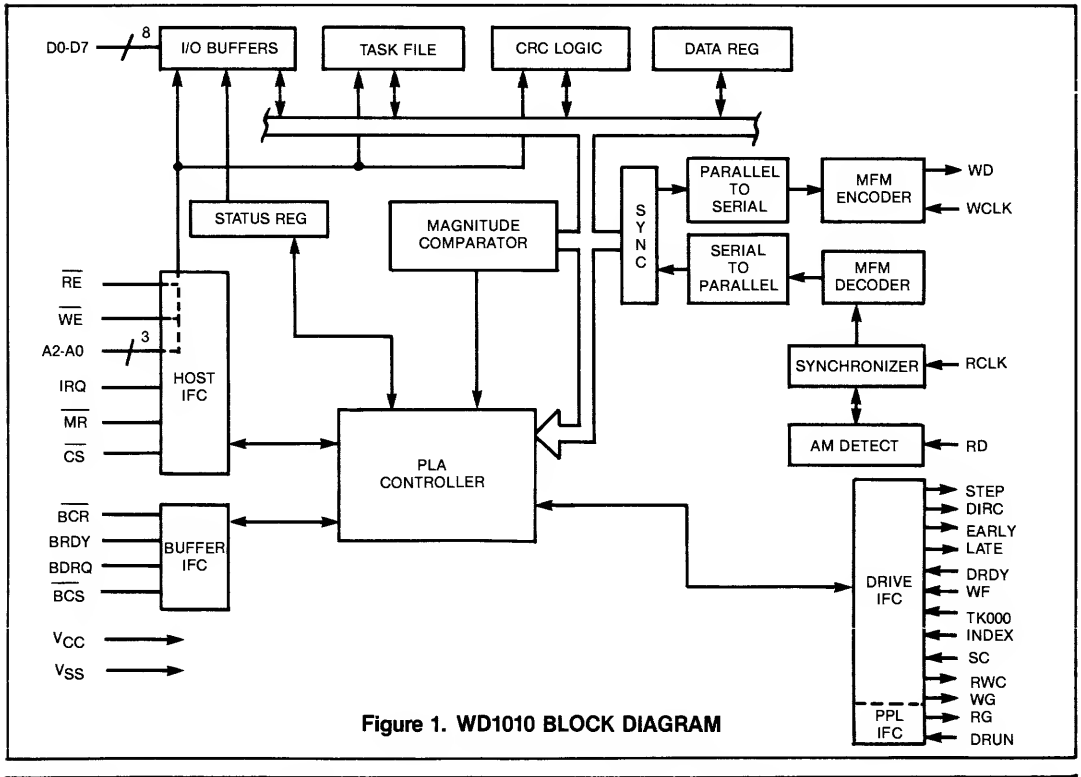


Figure 1. WD1010 BLOCK DIAGRAM

Host/Buffer IFC
This logic contains all of the necessary circuitry to communicate with the 8-bit host processor.

Drive IFC
This logic controls and monitors all lines from the drive, with the exception of read and write data.

DRIVE INTERFACE

The drive side of the WD1010 controller requires three sections of external logic. These are buffers/receivers, data separator, and write precompensation. Figure 2 illustrates a drive side interface.

The buffer/receivers condition the control lines to be driven down the cable to the drive. The control lines are typically single-ended, resistor terminated TTL levels. The data lines to and from the drive also require buffering, but are differential RS-422 levels. The interface specification to the drive can be found in the manufacturers' OEM manual. The WD1010 supplies TTL compatible signals, and will interface to most buffer/driver devices.

The data recovery circuits consist of a phase-lock loop data separator and associated components. The WD1010 interacts with the data separator through the DATA RUN (DRUN) and Read Gate (RG) signals. The block diagram of the data separator circuit is shown in Figure 3. Read data from the drive is presented to the RD input of the WD1010, the reference multiplexor, and a retriggerable one shot. The read gate (Pin 38) output will be low when the WD1010 is not inspecting data. The PLL at this time should remain locked to the reference clock.

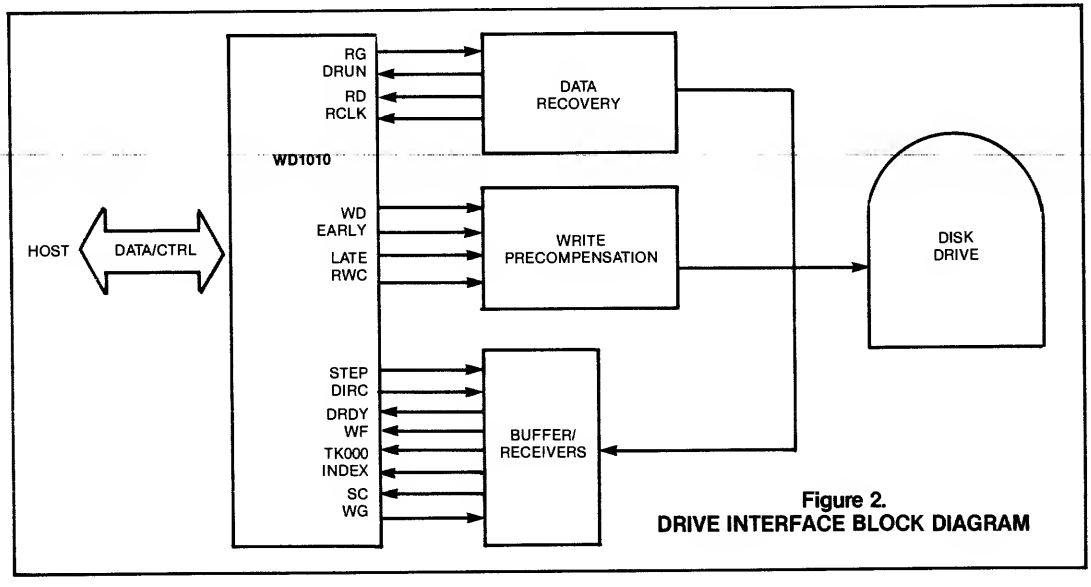


Figure 2.
DRIVE INTERFACE BLOCK DIAGRAM

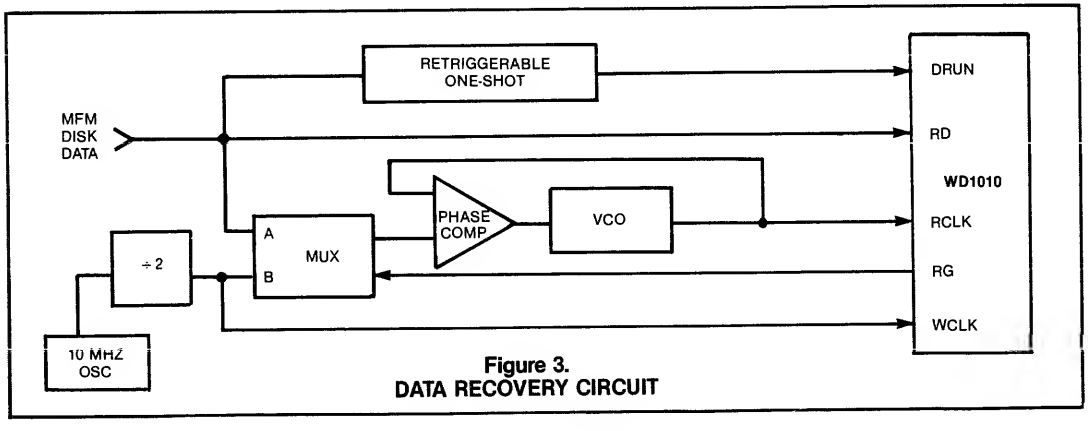


Figure 3.
DATA RECOVERY CIRCUIT

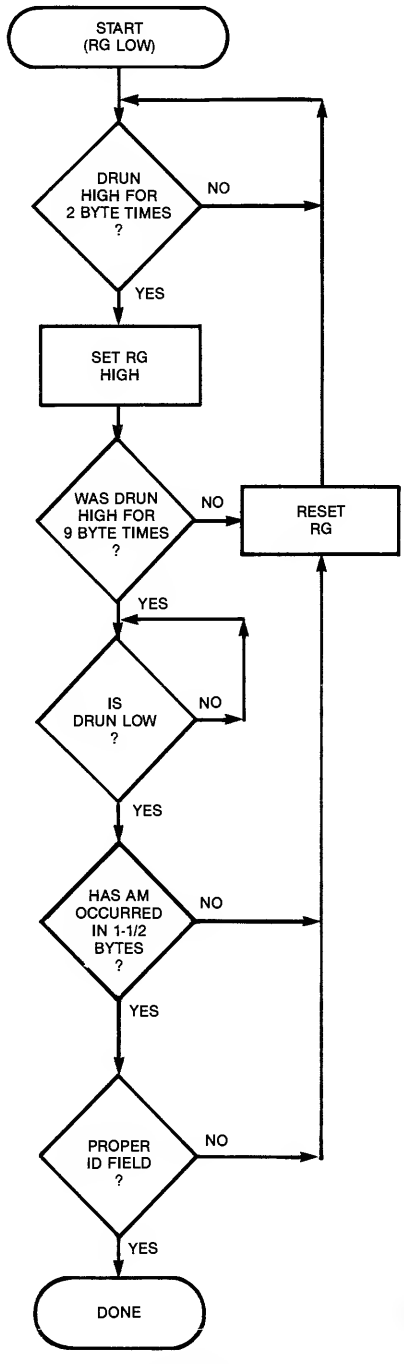


Figure 4.
PLL CONTROL SEQUENCE

When any Read/Write command is initiated and a search for address marks begins, the DRUN input is examined. The DRUN one-shot is set for slightly greater than one bit time, allowing it to retrigger constantly on a field of ones and zeros. An internal counter times out to see that DRUN is high for 16 bits (2 byte times). Since all address marks are preceded by 12 bytes of zeros, an attempt is made to read an address mark. If DRUN falls prior to 64 bit times, the process is repeated. Read gate is then set by the WD1010, switching the data separator to lock onto the incoming data stream. Read gate will remain active high until a non-zero, non-address mark byte is detected. It then will lower read gate for 2 byte times (to allow the PLL to lock back on the reference clock) and start the DRUN search over again. If an address mark is detected, read gate will be held high and the command will continue searching for the proper ID field. This sequence is shown in the flow chart of Figure 4.

The write precompensation logic is controlled by the signals Reduce Write Current (RWC), Early and Late. The cylinder in which the RWC line becomes active is controlled by a register in the Task File. It can be used to turn on the precomp circuitry on a predetermined cylinder.

The signals $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are used to tell the precomp how much delay is required on the write data pulse about to be sent. The amount of delay is determined externally through a digital delay line or equivalent circuitry. Since the signal $\overline{\text{Early}}$ occurs after the fact, write data should be delayed one interval when both Early and Late are high; two intervals when Late is low; and no delay when $\overline{\text{Early}}$ is low. An interval, for example, is 12-15 ns. on the ST506. $\overline{\text{Early}}$ or $\overline{\text{Late}}$ will be active slightly ahead of the write data pulse; Early and Late will never be low at the same time. Regardless of the contents of the RWC register, $\overline{\text{Early}}$ and $\overline{\text{Late}}$ will always be active.

Examples for all three of the above circuits can be found in the WD1010 Application Note.

HOST INTERFACE

The primary interface between the host processor and the WD1010 is through an 8-bit bidirectional bus. This bus is used to transmit/receive data to both the WD1010 and a sector buffer. The sector buffer is constructed with either FIFO memory or static RAM and a counter. Since the WD1010 will make the bus active when accessing the sector buffer, a transceiver must be used to isolate the host during this time. Figure 5 shows a typical connection to a sector buffer implemented with RAM memory. Whenever the WD1010 is not using the sector buffer, the Buffer Chip Select ($\overline{\text{BCS}}$) is high (disabled). This allows the host to access the WD1010's Task File, and to set up parameters prior to issuing a command. It also allows the host to access the RAM buffer. A decoder is used to generate a chip select when A_0-A_2 are '000'; an unused address in the WD1010. A binary counter is enabled whenever $\overline{\text{RE}}$ or $\overline{\text{WE}}$ goes active and in-

cremented on the trailing edge of the chip select. This allows the host to access sequential bytes within the RAM. The decoder also generates another chip select when A_0-$A_2 \neq$ '000'; allowing access to the WD1010's internal registers while keeping the RAM tri-stated.

During write sector commands, the processor sets up data in the Task File and issues the command. It then generates a status to inform the host it may load the buffer with the data to be written. When the counter reaches its maximum count, the Buffer Ready (BRDY) signal is made active (by the "carry" out of the counter), informing the WD1010 that the buffer is full. (BRDY is a rising edge activated signal.) The Buffer Chip Select ($\overline{BCS}$) is then made active, disconnecting the host through the transceivers, and the $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1010 to allow it access to the buffer. When the WD1010 is done using the buffer, it disables $\overline{BCS}$ which again allows host access to this local bus. The read sector commands operate in a similar matter, except the buffer is loaded by the WD1010 instead of the host.

Another control signal called Buffer Data Request (BDRQ; not used in Figure 5) is a DMA signal that can inform a direct memory access controller when the WD1010 is requesting data. For further explanation, refer to the description of the individual commands and the A.C. Timing Specifications. In a read command, interrupts are generated at the termination of a command; an interrupt may be specified to occur either at the end of the command or when BDRQ is activated. The interrupt line (INTRQ) is cleared either by reading the status register or by writing a new command in the command register.

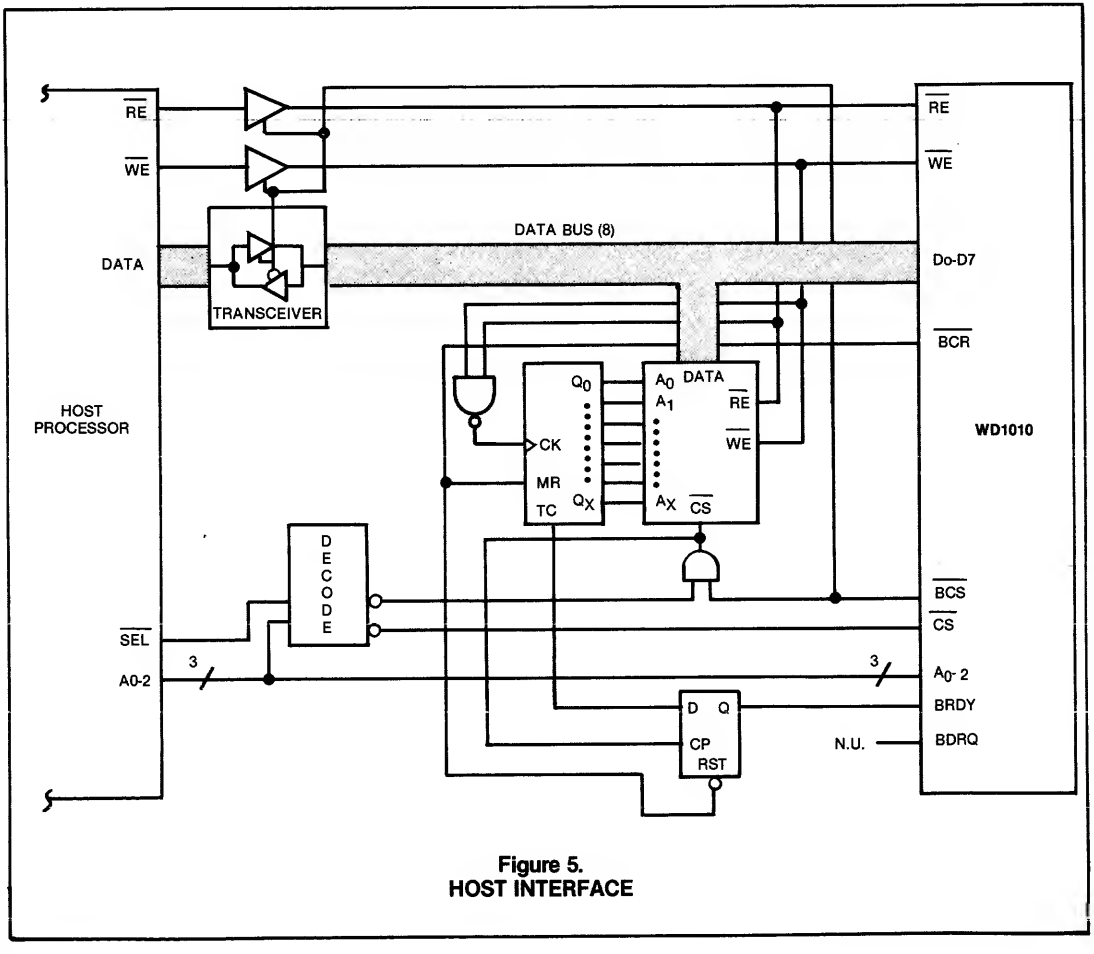


Figure 5.
HOST INTERFACE

TASK FILE

The Task File is a bank of registers used to hold parameter information pertaining to each command. These registers and their addreses are:

A_2	A_1	A_0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE: Registers are **not** cleared by master reset ($\overline{MR}$).

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC	—	ID	—	AC	TK	DM

Bit 7 — Bad Block Detect
This bit is set when an ID field has been encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 — CRC Data Field
This bit is set when a data field CRC error has occurred or the Data Address Mark has not been found. The sector buffer may still be read but will contain errors.

Bit 5 — Reserved
Not used; forced to a zero.

Bit 4 — ID Not Found
This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk, or if an ID field CRC error has occurred.

Bit 3 — Reserved
Not used; forced to a zero.

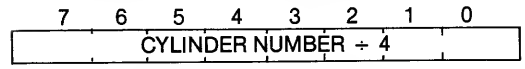
Bit 2 — Aborted Command
This bit is set if a command was issued while the DRDY (Pin 28) line is low or the WF (30) line is low. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 — TK000 Error
This bit is set only by the restore command. It indictes that the TK000 (Pin 31) line has not gone active after the issuance of 1024 stepping pulses.

Bit 0 — Data Address Mark Not Found
This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.

WRITE PRECOMP CYLINDER

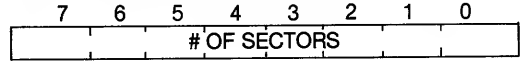
This register is used to define the cylinder number where the RWC (Pin 33) line is asserted:



The value (0-255) loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus, a value of H'01' will cause RWC to activate on cylinder 4; H'02' on cylinder 8, and so on. Switching points are then 0, 4, 8, . . . 1020. The RWC will be asserted when the present cylinder is equal to a greater than the value in this register. For example, the ST506 requires precomp on cylinder 128 (H'80') and above. Therefore, the write precomp cylinder register should be loaded with 32 (H'20').

SECTOR COUNT

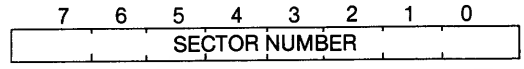
This register holds the number of sectors that are needed to be transferred to the buffer:



This register is used during a multiple sector R/W command. The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

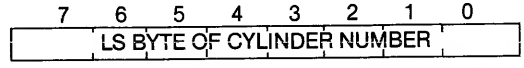
This register holds the sector number of a desired sector:



During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from 0 to 255.

CYLINDER NUMBER LOW

This register holds the least significant 8 bits of the desired cylinder number:



It is used in conjunction with the cylinder number high register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH

This register defines the two most significant bits of the cylinder number desired:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	(9)	(8)

Internal to the WD1010, is another pair of registers that hold the actual position number where the R/W heads are located. The cylinder number high and low registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WD1010 automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a Restore.

SDH BYTE

This register contains the desired sector size, drive number, and head number parameters. The format is:

7	6	5	4	3	2	1	0
EXT	SIZE		DRIVE		HEAD		

6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

Both head number and sector size is compared against the disks' ID field. Head select and drive select lines are not available as outputs from the WD1010, and must be generated externally. Figure 6 shows the logic to implement these select lines.

Bit 7, the extension bit, is used to extend the data field by seven bytes when using ECC codes. CRC is not appended to the end of the data field when EXT = 1; the data field becomes "sector size +7" bytes long. CRC is checked on the ID field regardless of the state of the extension bit. Note that the sector size bits are written to the ID during a formatting command. The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written but does have bad block mark written. The format is:

BAD BLOCK	SIZE	0	0	HEAD #			
7	6	5	4	3	2	1	0

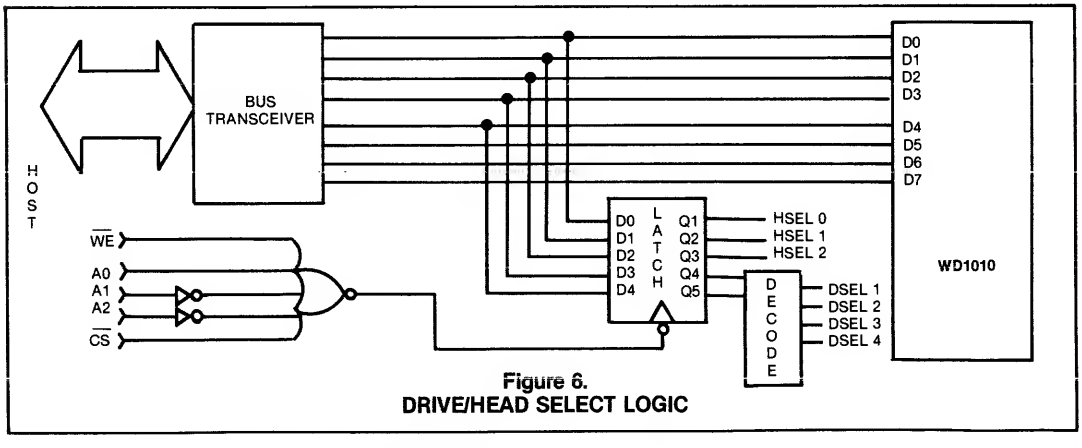


Figure 6.
DRIVE/HEAD SELECT LOGIC

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the WD1010 as well as reporting status from the drive control lines. The format is:

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	—	CIP	ERR

Bit 7 — Busy
This bit is set whenever the WD1010 is accessing the disk. Commands should not be loaded into the command register while busy is set. Busy is made active when a command is written into the WD1010 and is deactivated at the end of all commands except the read sector. While executing a read sector command, busy is deactivated after the sector buffer has been filled.

Bit 6 — Ready
This pin normally reflects the state of the DRDY (Pin 28) line.

Bit 5 — Write Fault
This bit reflects the state of the WF (Pin 30) line. Whenever the WF pin goes high, an interrupt will be generated.

Bit 4 — Seek Complete
This bit reflects the state of the SC (Pin 32) line. Certain commands will pause until seek complete is true.

Bit 3 — Data Request
This bit reflects the state of the BDRQ (Pin 36) line. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command. DRQ/BDRQ remains high until BRDY is sensed, indicating the operation is completed. The BDRQ signal can be used in DMA interfacing, while the DRQ bit can be used for programmed I/O transfers.

Bit 2 — Reserved
Not used. This bit is always forced to a zero.

Bit 1 — Command in Progress
When this bit is set, a command is being executed and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host.

Bit 0 — Error
This bit is set whenever any bits in the error register are set. It is the logical 'or' of the error register and may be used by the host to quickly check successful completion of a command. This bit is reset when a new command is written into the command register.

COMMAND REGISTER

This write-only register is loaded with desired command:

7	6	5	4	3	2	1	0
COMMAND							

The commands begins to execute immediately upon loading. This register should not be loaded while the Busy or CIP bits are set in the status register. The INTRQ (Pin 3) line, if set, will be cleared by a write to the command register.

INSTRUCTION SET

The WD1010 will execute six commands. Prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

COMMAND SUMMARY

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R_3	R_2	R_1	R_0
SEEK	0	1	1	1	R_3	R_2	R_1	R_0
READ SECTOR	0	0	1	0	I	M	0	0
WRITE SECTOR	0	0	1	1	0	M	0	0
SCAN ID	0	1	0	0	0	0	0	0
WRITE FORMAT	0	1	0	1	0	0	0	0

R_3-R_0 Rate Field

For 5 MHz WCLK:
R_3-R_0 = 0000 — ≈35 μs.
0001 — .5 ms.
0010 — 1.0 ms.
0011 — 1.5 ms.
0100 — 2.0 ms.
0101 — 2.5 ms.
0110 — 3.0 ms.
0111 — 3.5 ms.
1000 — 4.0 ms.
1001 — 4.5 ms.
1010 — 5.0 ms.
1011 — 5.5 ms.
1100 — 6.0 ms.
1101 — 6.5 ms.
1110 — 7.0 ms.
1111 — 7.5 ms.

Bit 0, ("T") Read Sector, Write Sector Commands

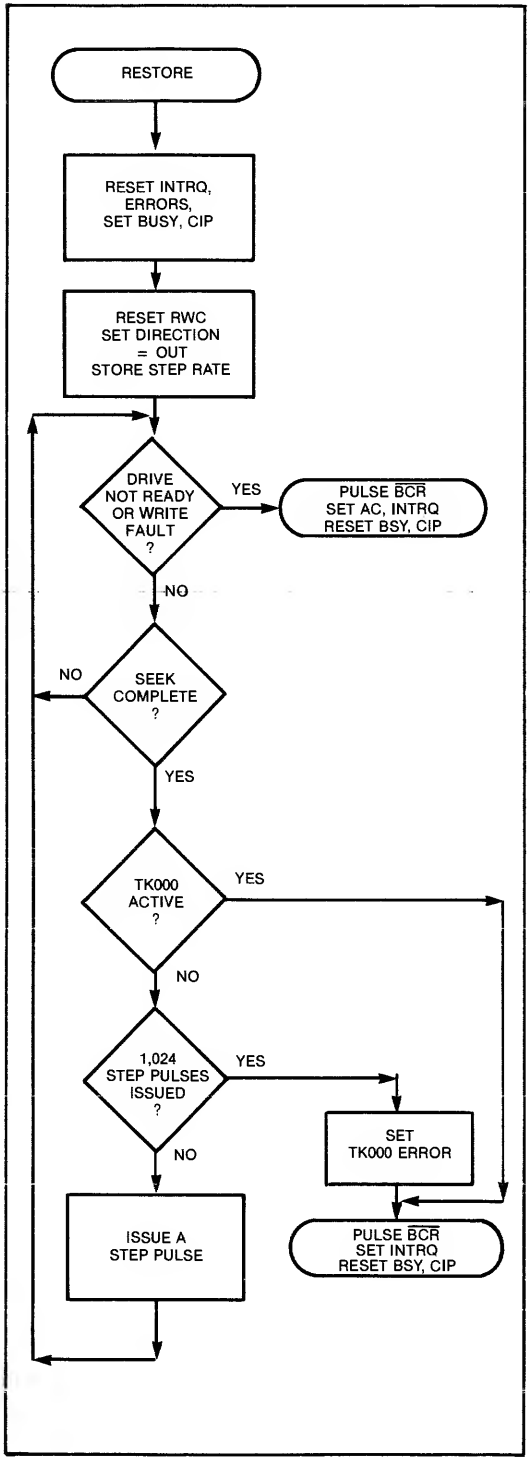
Should be set to 0 for WD1010-00
Should be set to 1 for WD1010-01

M = Multiple Sector Flag

M = 0 Transfer 1 sector
M = 1 Transfer multiple sectors

I = Interrupt Enable

I = 0, Interrupt at BDRQ time
I = 1, Interrupt at end of command



RESTORE COMMAND

The restore command is usually used on a power-up condition. The actual stepping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1010 waits for the Seek Complete line to go active before issuing the next pulse. If after 1,024 stepping pulses, the TK000 line does not go active, the WD1010 will set the TK000 error bit in the error register and terminate with an INTRQ. An interrupt will also occur if the write fault goes active or the DRDY goes inactive during execution.

The rate field specified (R_3-R_0) is stored in an internal register for future use in commands with implied seeks.

SEEK COMMAND

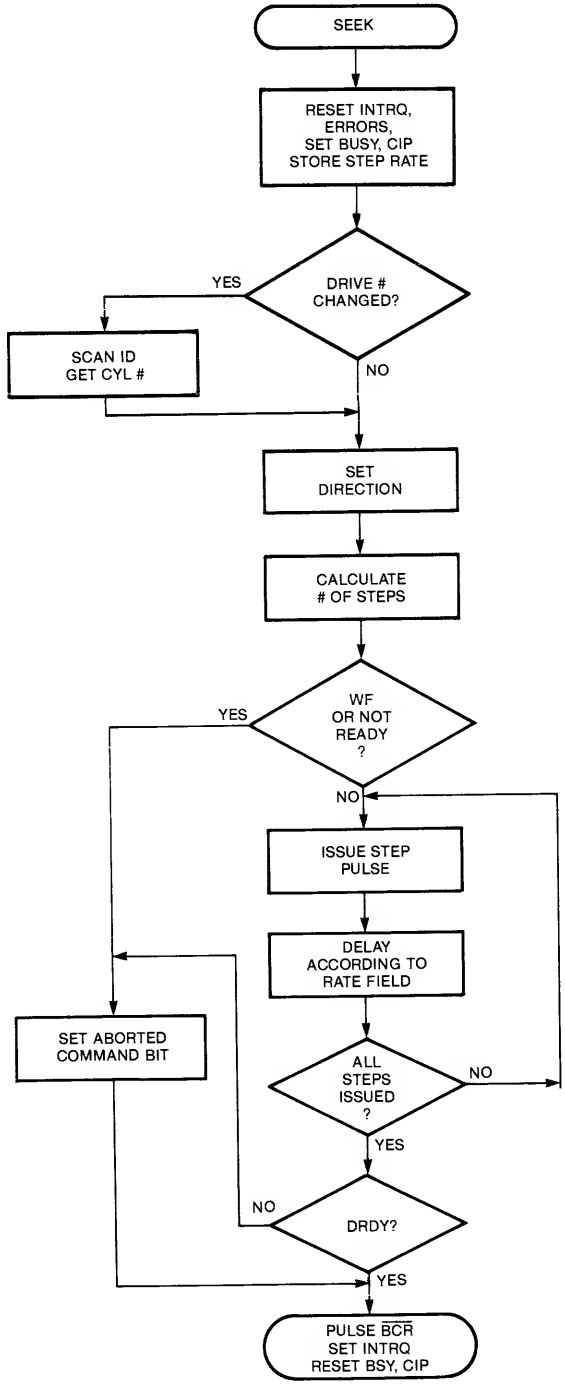
Since all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The actual step rate used is taken from the rate field, which is also stored in an internal register for future use. If DRDY goes inactive or WF goes active, the command is terminated and an INTRQ is generated.

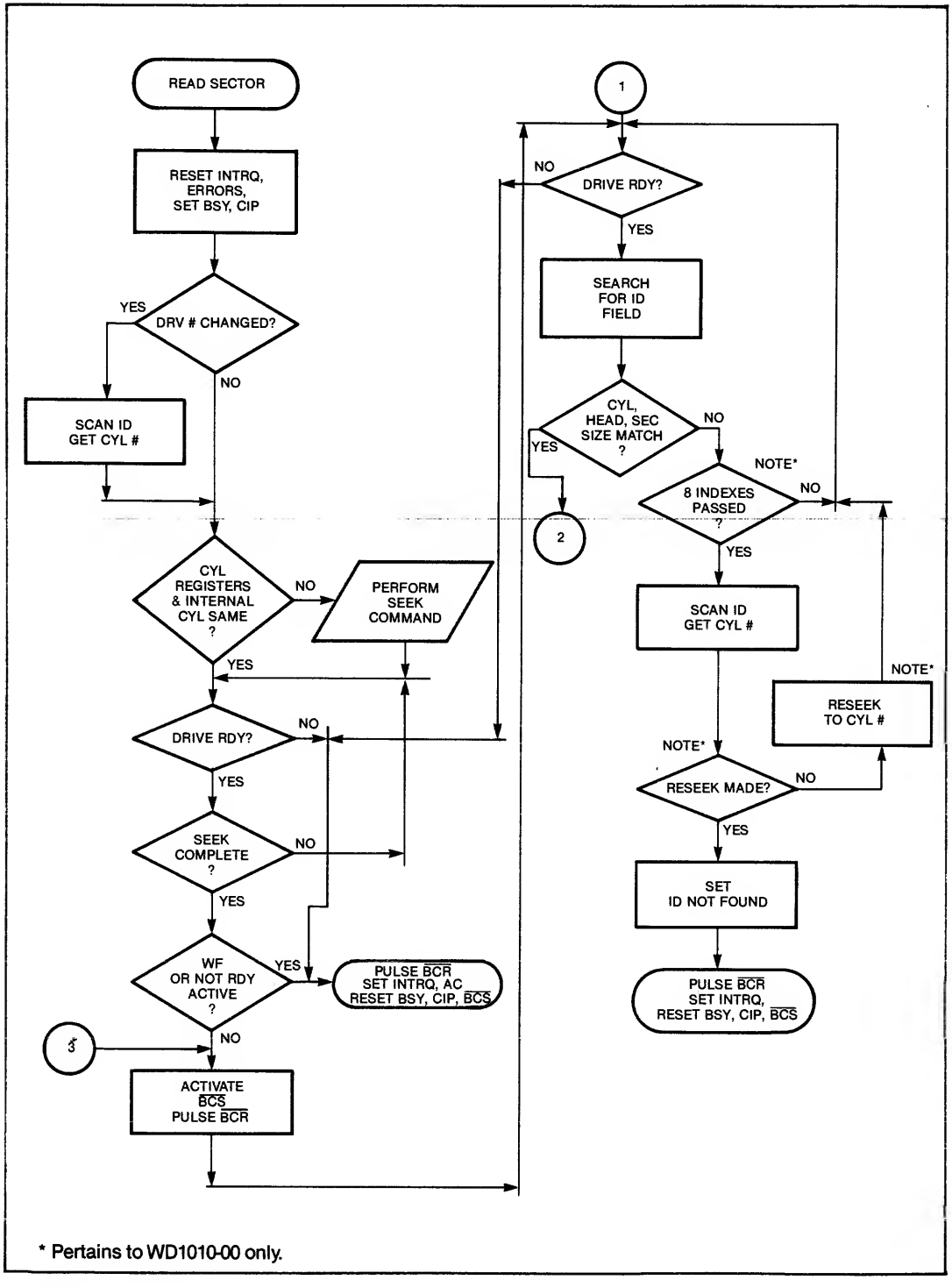
The direction and number of step pulses needed are calculated by comparing the contents of the cylinder register high/low to the cylinder position number stored internally. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. Seek complete is not checked at the beginning or end of the command.

READ SECTOR

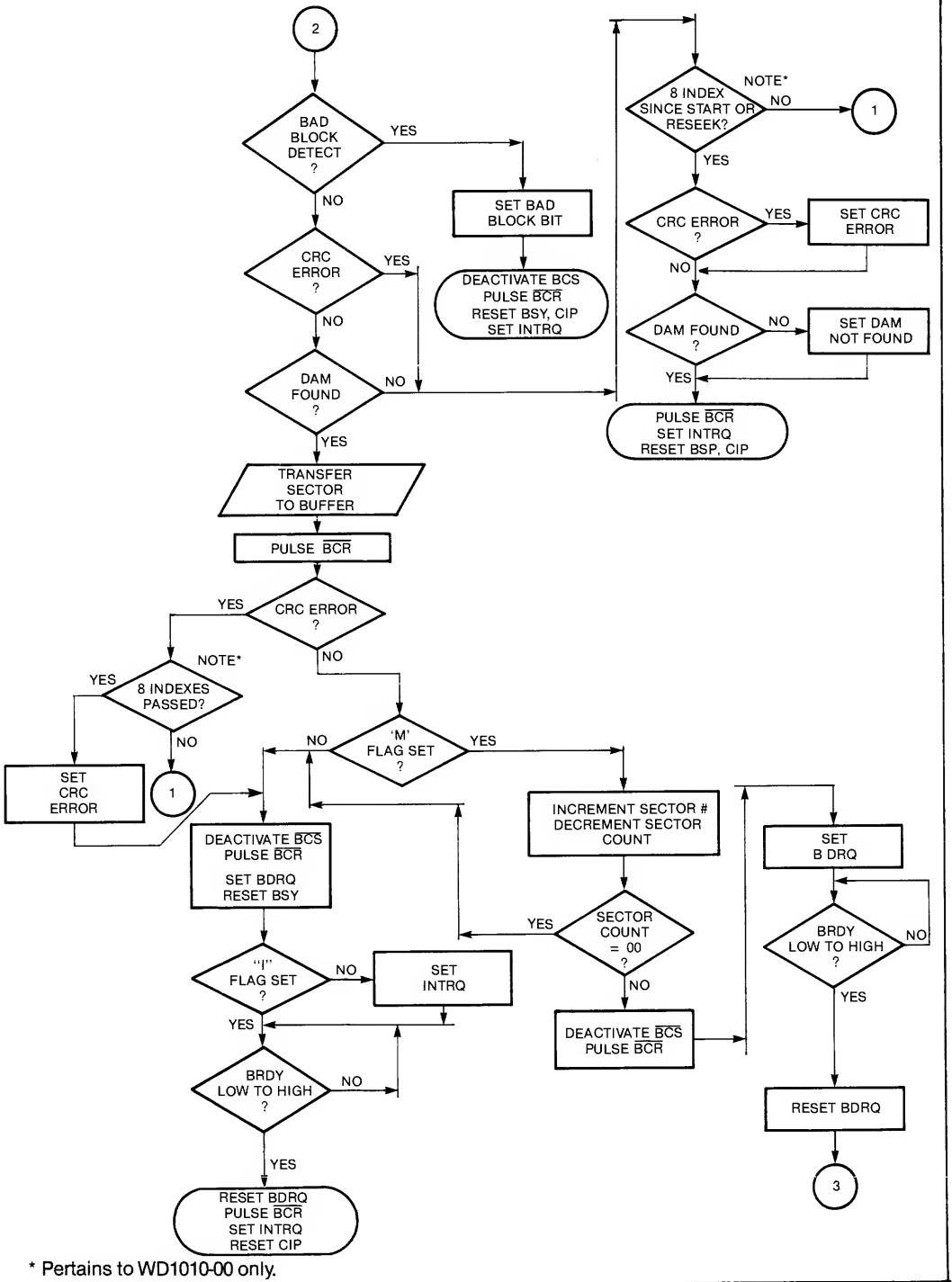
The read sector command is used to transfer one or more sectors of data to the disk. Upon receipt of this command, the WD1010 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and a seek takes place. Write Fault and DRDY lines are checked throughout the command.

After seek complete is found to be true (with or without an implied seek), the search for an ID field occurs. The WD1010-00 must find an ID with the correct cylinder, head, sector size, and CRC within 8 revolutions; else the appropriate error bits will be set and the command terminated. If not, eight retries are performed with the ID-NOT-FOUND error bit set and the command terminated. Both the Read and Write sector commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command.


SEEK
RESET INTRQ, ERRORS, SET BUSY, CIP STORE STEP RATE
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SET DIRECTION
CALCULATE # OF STEPS
WF OR NOT READY ?
YES
NO
ISSUE STEP PULSE
DELAY ACCORDING TO RATE FIELD
SET ABORTED COMMAND BIT
ALL STEPS ISSUED ?
NO
YES
DRDY?
NO
YES
PULSE BCR
SET INTRQ
RESET BSY, CIP



* Pertains to WD1010-00 only.



* Pertains to WD1010-00 only.

When the data address mark is found, the WD1010 is ready to transfer data to the buffer. After the sector data has been transferred, the I flag is checked. If the I flag is 0, the INTRQ is made active coincident with BDRQ, indicating a transfer of data is required by the host. If I = 1, the INTRQ will occur at the end of the command (i.e. after the buffer is unloaded by the host).

An optional M flag may be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1010 decrements the sector count register and increments the sector number register. The next logical sector will be transferred, regardless of the interleave. Sectors are numbered at format time by a byte in the ID field.

For the WD1010 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. The sector transfers will continue until the sector count register equals zero or BRDY goes inactive. If the sector count register is non-zero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the next sector in this multiple sector read command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(5)	1010:	Sets BDRQ = 1; sets DRQ flag.
(6)	1010:	If I bit = 1 then (9).
(7)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$).
(8)	1010:	Waits for BDRY then sets INTRQ = 1; End.
(9)	1010:	Sets INTRQ = 1.
(10)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$); End.

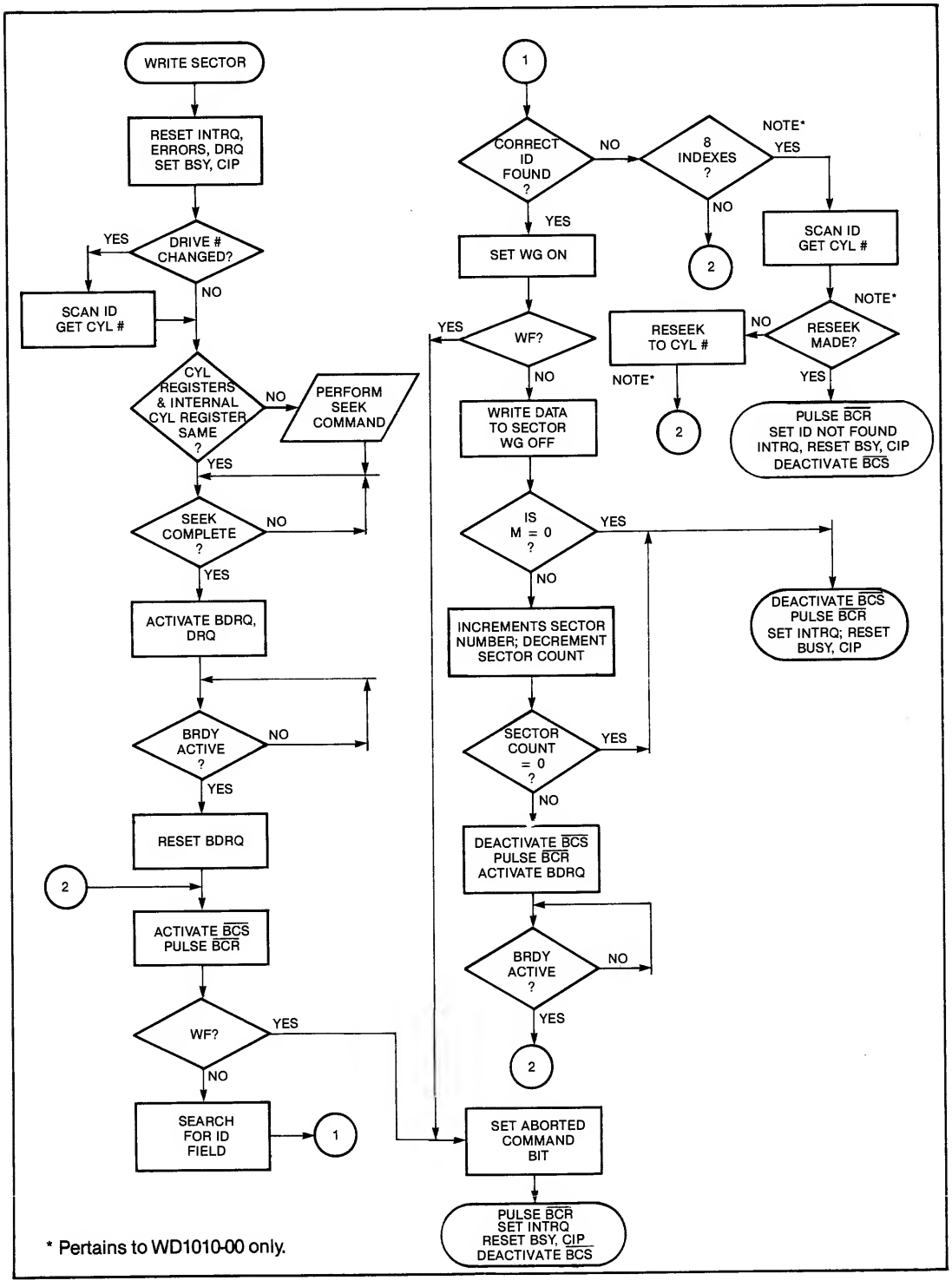
When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; set $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Decrements sector count register; increments sector number register.
(5)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(6)	1010:	Sets BDRQ = 1; DRQ flag = 1.
(7)	Host:	Reads out content of buffer (by $\overline{RE}$ strobes).
(8)	Buffer:	Indicates data has been transferred by asserting BRDY.
(9)	1010:	When BRDY is asserted, go to (11) if sector count = 0.
(10)	1010:	Go to Step (2).
(11)	1010:	Activates INTRQ.

WRITE SECTOR

The write sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1010 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a seek command takes place. Write fault and DRDY lines are checked throughout the command.

After Seek complete is found to be true (with or without an implied seek), the BDRQ signal is made active and the host proceeds to load the buffer. When the WD1010 senses the BRDY line going high, the ID field with the specified cylinder, head, and sector size is searched for. Once found, the write gate signal is raised and the data is written to the disk. If the ID field cannot be found within 8 revolutions, the ID not found bit is set and the command is terminated.


WRITE SECTOR
RESET INTRQ, ERRORS, DRQ SET BSY, CIP
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
CYL REGISTERS & INTERNAL CYL REGISTER SAME ?
NO
PERFORM SEEK COMMAND
YES
SEEK COMPLETE ?
NO
YES
ACTIVATE BDRQ, DRQ
BRDY ACTIVE ?
NO
YES
RESET BDRQ
2
ACTIVATE BCS PULSE BCR
WF?
YES
NO
SEARCH FOR ID FIELD
1
1
CORRECT ID FOUND ?
NO
8 INDEXES ?
NOTE*
YES
NO
2
SCAN ID GET CYL #
SET WG ON
YES
WF?
NO
NOTE*
RESEEK TO CYL #
NO
RESEEK MADE?
NOTE*
YES
2
PULSE BCR SET ID NOT FOUND INTRQ, RESET BSY, CIP DEACTIVATE BCS
WRITE DATA TO SECTOR WG OFF
IS M = 0 ?
YES
NO
DEACTIVATE BCS PULSE BCR SET INTRQ; RESET BUSY, CIP
INCREMENTS SECTOR NUMBER; DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
DEACTIVATE BCS PULSE BCR ACTIVATE BDRQ
BRDY ACTIVE ?
NO
YES
2
SET ABORTED COMMAND BIT
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
* Pertains to WD1010-00 only.

During a multiple sector write operation (M flag = 1), the sector number is incremented and the sector count register is decremented. If the BRDY line is asserted after the first sector is read out of the buffer, the WD1010-00/01 will continue to read data out of the buffer for the next sector. If BRDY is inactive, the WD1010-00/01 will raise BDRQ and wait for the host to place more data in the buffer.

In summary then, the write sector operation is as follows:

(1)	Host:	Sets up parameters; issues write sector command.
(2)	1010:	Sets BDRQ = 1, DRQ flag = 1.
(3)	Host:	Loads buffer with data (by WE strobes).
(4)	1010:	Waits for BRDY = low to high.
(5)	1010:	Finds specified ID field, write out sector.
(6)	1010:	If M = 0, then interrupt; End.
(7)	1010:	Increments sector number, decrements sector count.
(8)	1010:	If sector count = 0, then interrupt; End.
(9)	1010:	Go to (2).

SCAN ID

The scan ID command is used to update the head, sector size, sector number and cylinder registers.

The ready and write fault lines are checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, cylinder, and sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, the WD1010 will retry up to 8 revolutions to find an error-free ID field. There is no implied seek with this command and the buffer is left undisturbed.

FORMAT

The format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 7 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A H'00' is normal; a H'80' indicates a bad block mark for that sector. In the example of Figure 7, sector 04 will get a bad block mark recorded.

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY to tell the WD1010 to begin formatting the track.

An implied seek is also in effect on this command. As in other commands, if the drive number has changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incompatible format had been used), an IDNF error will result and the Format command will be aborted. This can be avoided by issuing a Restore command before formatting.

The sector count register is used to hold the total number of sectors to be formatted, while the sector number register holds the number of bytes minus 3 to be used for Gap 1 and Gap 3; for instance, if the sector count register value is 2 and the sector number register value is 0, then 2 sectors are written and 3 bytes of H'4E' are written for Gap 1 and Gap 3.

	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
:				:				
:				:				
F0	FF	FF	FF	FF	FF	FF	FF	FF

Figure 7.
FORMAT COMMAND BUFFER CONTENTS

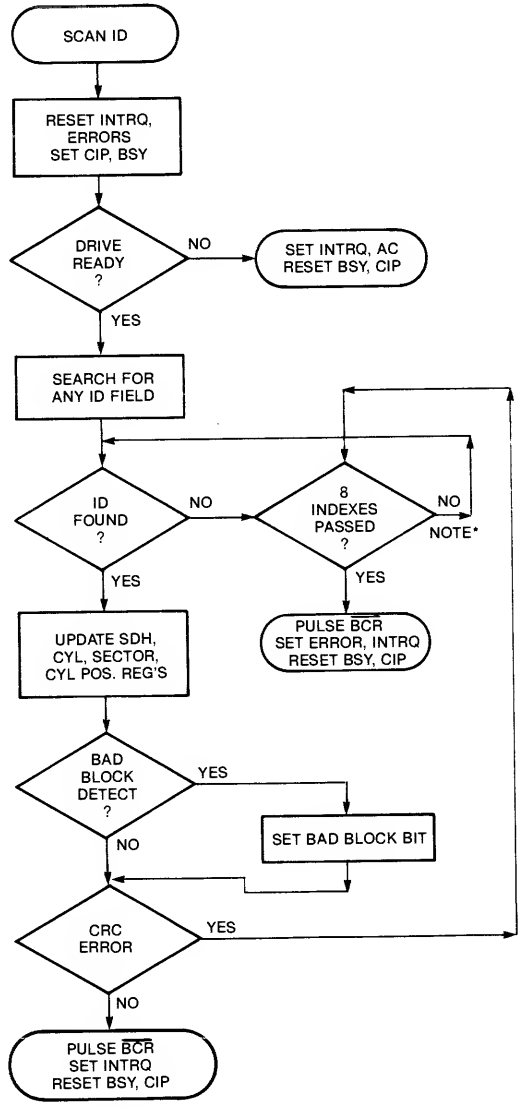
The data fields are filled with H'FF,' and CRC is automatically generated and appended. The sector extension bit of the SDH register should not be set. After the last sector is written, H'4E' is filled until index. Like all commands, a write fault or drive not ready condition will terminate the command. Figure 8 shows the format that the WD1010 will write on the disk.

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining the minimum Gap 3 value is:

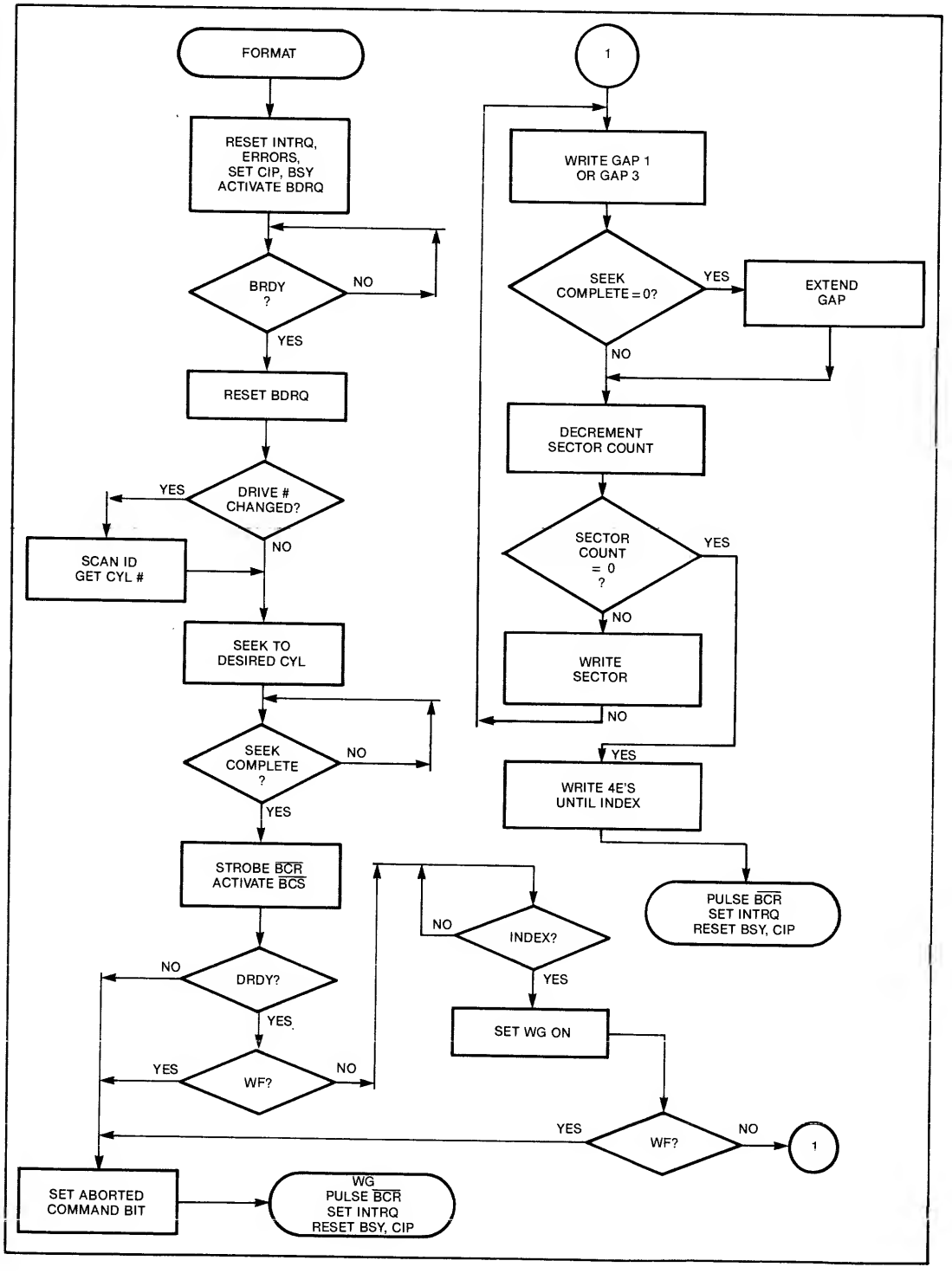
Gap 3 = 2*M*S + K + E

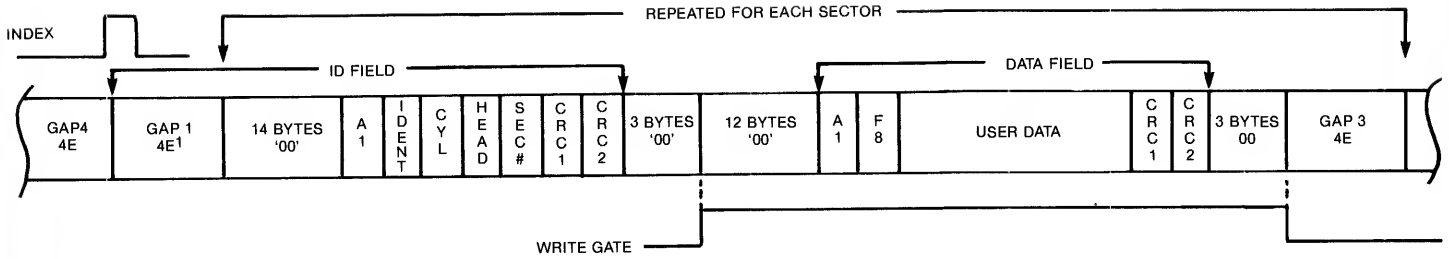
M = motor speed variation (e.g. .03 for + – 3%)
S = sector length in bytes
K = 25 for interleave factor of 1
K = 0 for any other interleave factor
E = 7 if the sector is to be extended

Like all commands, a write fault or not ready condition will terminate the command. Figure 8 shows the format that the WD1010 will write on the Disk.



* Pertains to WD1010-00 only.


FORMAT
RESET INTRQ, ERRORS, SET CIP, BSY ACTIVATE BDRQ
BRDY ?
NO
YES
RESET BDRQ
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SEEK TO DESIRED CYL
SEEK COMPLETE ?
NO
YES
STROBE BCR ACTIVATE BCS
DRDY?
NO
YES
WF?
YES
NO
SET ABORTED COMMAND BIT
WG PULSE BCR SET INTRQ RESET BSY, CIP
1
WRITE GAP 1 OR GAP 3
SEEK COMPLETE = 0?
YES
EXTEND GAP
NO
DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
WRITE SECTOR
NO
YES
WRITE 4E'S UNTIL INDEX
PULSE BCR SET INTRQ RESET BSY, CIP
INDEX?
NO
YES
SET WG ON
WF?
YES
NO
1



ID FIELD

A1 = H'A1' with H'0A' clock.

IDENT = MSB of Cylinder Number
FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512-767 Cylinders
FD = 768-1023 Cylinders

HEAD = Bits 0, 1, 2 = Head Number
Bits 3, 4 = 0
Bits 5, 6 = Sector Size
Bit 7 = Bad Block Mark

Sec # = Logical Sector Number

DATA FIELD

A1 = H'A1' with H'0A' Clock

F8 = Data Address Mark; Normal Clock

USER = Data Field 128 to 1024 Bytes[2]

NOTES:
1. GAP1 and 3 length determined by sector number register contents during formatting.
2. If EXT bit in SDH register is set to 1 then an additional 7 data bytes are written, no CRC bytes are written.

Figure 8.
FORMAT

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with
respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

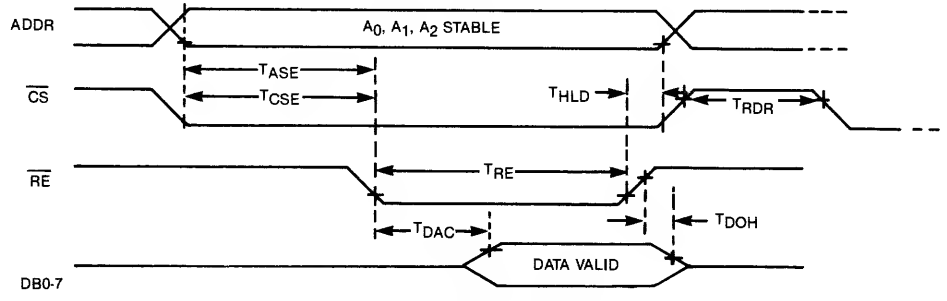
DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		± 10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Drain)		± 10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = −100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
V_{OL}	Output Low Voltage (Pins 21-23)		0.45	V	IO = 4.8 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	For Pins 25, 34, 37, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise Time		30	ns	10% to 90% points

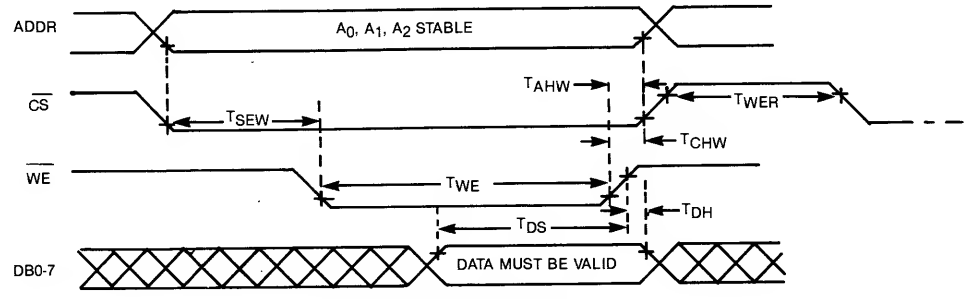
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{ASE}	ADDR Setup to $\overline{RE}$	100		ns	
T_{DAC}	Data Valid from $\overline{RE}$		375	ns	
T_{RE}	Read Enable Pulse Width	.4	10	μs	
T_{DOH}	Data Hold from $\overline{RE}$	20	200	ns	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		ns	
T_{RDR}	Read Recovery Time	300		ns	
T_{CSE}	$\overline{CS}$ Setup To	0		ns	



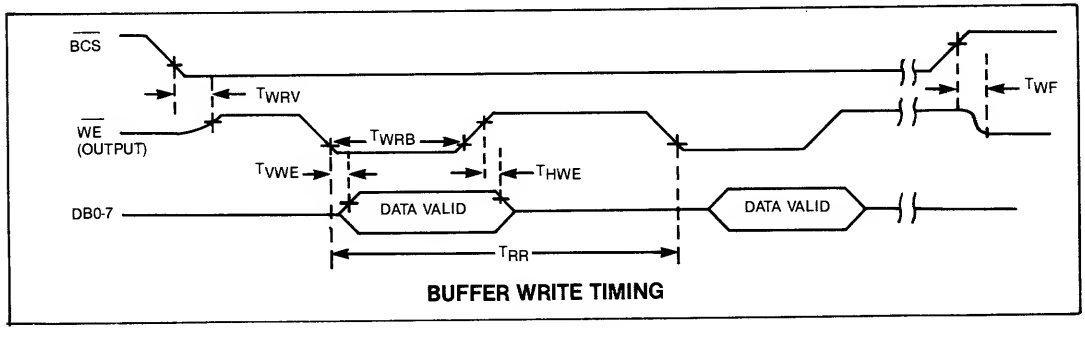
HOST READ TIMING



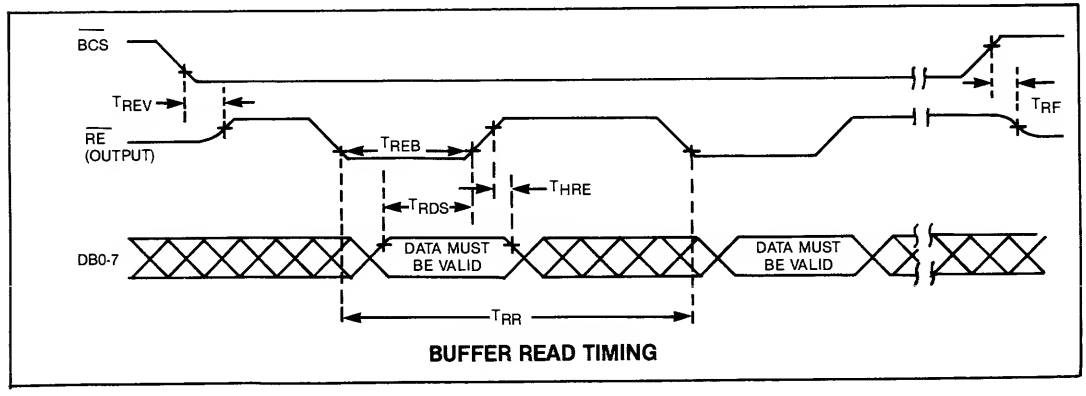
HOST WRITE TIMING

HOST WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SEW}	ADDR, $\overline{CS}$ Setup to $\overline{WE}$	0	10	μs	
T_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	μs	
T_{WE}	Write Enable Pulse Width	.2	10	μs	
T_{DH}	Data Bus Hold from $\overline{WE}$	10		ns	
T_{AHW}	ADDR Hold from $\overline{WE}$	30		ns	
T_{WER}	Write Recovery Time	1.0		μs	See Note 1
T_{CHW}	$\overline{CS}$ Hold Time	0			



BUFFER WRITE TIMING



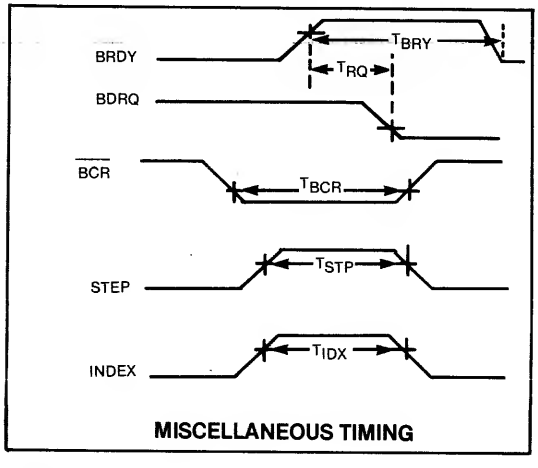
BUFFER READ TIMING

BUFFER WRITE TIMING (READ SECTOR CMD)

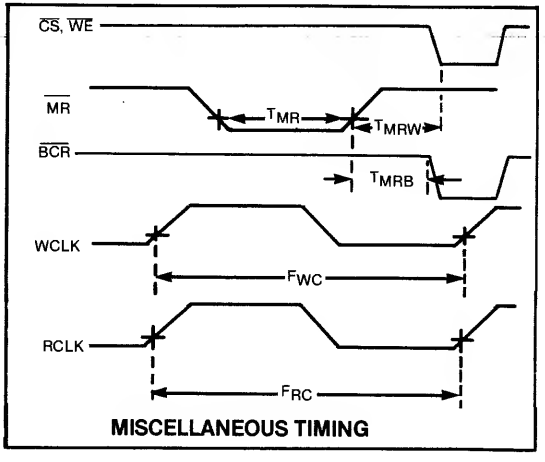
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	ns	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{VWE}	Data Valid from $\overline{WE}$			110	ns	
T_{HWE}	Data Hold from $\overline{WE}$	60			ns	
T_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	µs	See Note 2
T_{WF}	$\overline{WE}$ Float from BCS	15		100	ns	C_L = 50 pf

BUFFER READ TIMING (WRITE SECTOR CMD)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	ns	C_L = 50 pf
T_{REB}	RE Output Pulse Width	300	400	500	ns	See Note 4
T_{RDS}	Data Setup to $\overline{RE}$	140			ns	
T_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	µs	See Note 2
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	ns	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			ns	



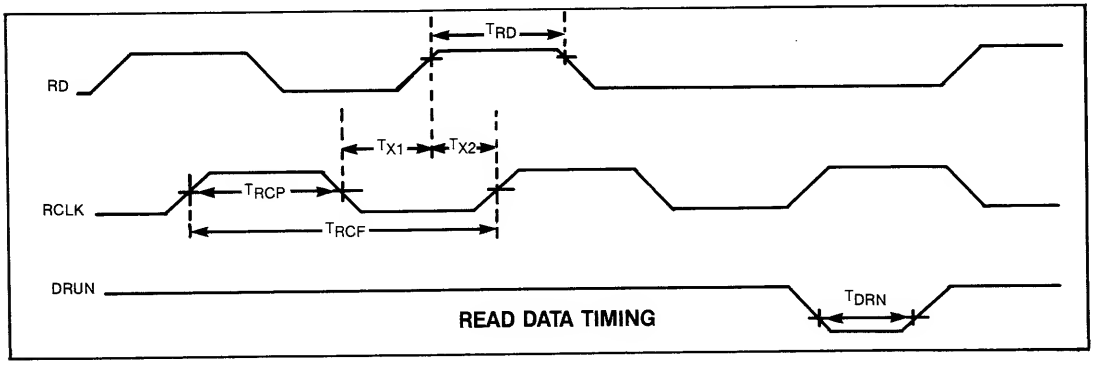
MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

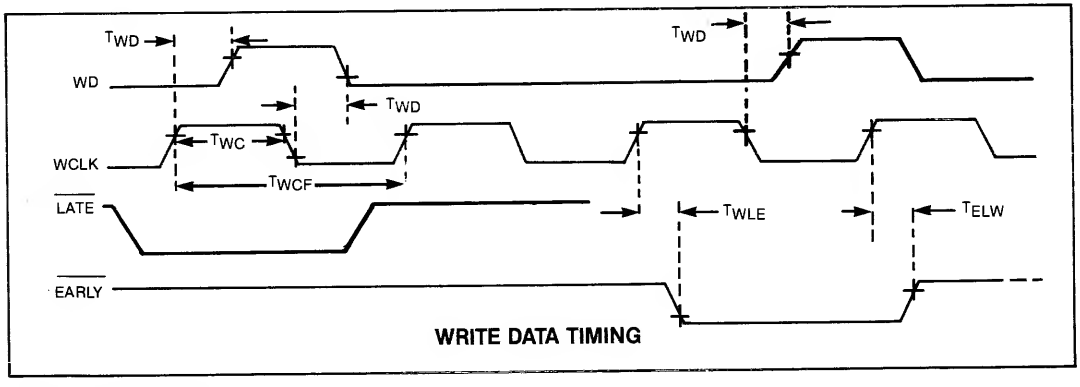
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RQ}	BDRQ Reset from BRDY	40		200	ns	
T_{BCR}	Buffer Counter Reset Pulse Width	1.4	1.6	1.8	µs	See Note 2
T_{STP}	Step Pulse Width	8.3	8.4	8.7	µs	See Note 2
T_{IDX}	Index Pulse Width	5		15	µs	
T_{MR}	Master Reset Pulse Width	24			WC	See Note 3
F_{WC}	Write Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
F_{RC}	Read Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
T_{BRY}	BRDY Pulse Width	800			ns	See Note 5
T_{MRB}	$\overline{MR}$ Trailing To $\overline{BCR}$	1.6	3.2	6.4	µs	See Note 2
T_{MRW}	$\overline{MR}$ Trailing To Host Write	6.4			µs	See Note 2



READ DATA TIMING

READ DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	95		2000	ns	50% Duty Cycle
T_{X1}	RD from RCLK Transition	0		$T_{RCP} \div 2$	ns	
T_{X2}	RD to RCLK Transition	20		$T_{RCP} \div 2$	ns	
T_{RD}	RD Pulse Width	40		T_{RCP}	ns	
T_{DRN}	DRUN Pulse Width	30			ns	
T_{RCF}	RCLK Frequency	.250		5.25	MHZ	See Note 6



WRITE DATA TIMING

WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	ns	
T_{WD}	Prepagation Delay WCLK to WD	10		65	ns	
T_{WLE}	WCLK to Leading Early/Late	10		65	ns	
T_{ELW}	WCLK to Trailing Early/Late	10		65	ns	
T_{WCF}	WCLK Frequency	.250		5.25	MHZ	See Note 6

NOTES:
1. AC timing measured at $V_{OH} = 2.0V$, $V_{OL} = 0.8V$, $C_L = 50$ pf.
2. Based on WCLK = 5.0 MHz.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz).
4. 2 WCLK ± 100 ns.
5. BRDY must be >4 μs or a spurious BDRQ pulse may exist for up [illegible] μs after rising edge of BRDY.
6. $T_{RCF} = T_V$ [illegible] ± 15%.

See page 481 for ordering information.

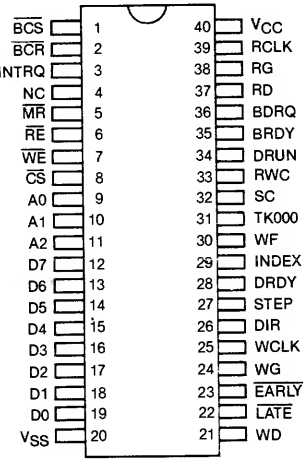
Printed in U.S.A

PRELIMINARY

WD1010-05/08 Winchester Disk Controllers

FEATURES

- ST506/SA1000 COMPATIBLE
- MULTIPLE SECTOR READ/WRITE
- UP TO 5MBITS/SEC DATA RATE
- UNLIMITED SECTOR INTERLEAVE
- AUTOMATIC FORMATTING
- CRC/ECC CAPABILITY WITH EXTERNAL ECC GENERATOR/CHECKER
- PROGRAMMABLE RETRIES
- VARIABLE SECTOR SIZE
- SINGLE +5V SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1010-05/08 is a MOS/LSI device which performs the functions of a Winchester Disk Controller/Formatter. It is compatible with the Seagate ST506 and the Shugart Associates SA1000 drives, as well as all other 5¼" and 8" products utilizing the same type of interface. On the host side, an 8 bit bi-directional bus accepts all commands, data, and status bytes. The Western Digital WD1000 series of board level controllers are software compatible with the WD1010-05/08.

Operating from a single 5 volt supply, the WD1010-05/08 is implemented in NMOS silicon gate technology and is available in a 40 pin dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
12-19	DATA 7 - DATA 0	D7-D0	Eight bit tristate bidirectional bus used for transfer of commands, status, and data.
6	READ ENABLE	$\overline{RE}$	Tristate bidirectional line, used as an input for reading the task register and an output when WD1010-05/08 is reading the buffer.
7	WRITE ENABLE	$\overline{WE}$	Tristate bidirectional line used as an input for writing into the task register and as an output when the WD1010-05/08 is writing to the buffer.
9-11	ADDRESS 0 - ADDRESS 2	A0-A2	These three inputs select the register to receive/transmit data on D0-D7.
8	CHIP SELECT	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
3	INTERRUPT REQUEST	INTRQ	Active high output which is set to a logic high in the completion of any command.
5	MASTER RESET	$\overline{MR}$	A logic low in this input will initialize all internal logic.
1	BUFFER CHIP SELECT	$\overline{BCS}$	Active low output used to enable reading or writing of the external sector buffer.
35	BUFFER READY	BRDY	This rising edge activated input is used to inform the controller that the sector buffer is full or empty.
2	BUFFER COUNTER RESET	$\overline{BCR}$	Active low output that is strobed by the WD1010-05/08 prior to read/write operations. This pin is strobed whenever $\overline{BCS}$ changes state.
36	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the sector buffer.
40	+5 VOLT	V_{CC}	+5V ±5% Power supply input.
20	GROUND	V_{SS}	Ground
4	NO CONNECT	NC	
21	WRITE DATA	WD	This output contains the MFM clock and data pulses to be written on the disk.
25	WRITE CLOCK	WCLK	4.34 or 5.0 Mhz clock input used to derive all internal write timing.
24	WRITE GATE	WG	This output is set to a logic high before writing is to be performed on the disk.
23, 22	EARLY, LATE	$\overline{EARLY}$, $\overline{LATE}$	Precompensation outputs used to delay the WD pulses externally.
37	READ DATA	RD	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
39	READ CLOCK	RCLK	A nominal square wave clock input derived from the external data recovery circuits.
38	READ GATE	RG	This output is set to a logic high when data is being inspected from the disk.
34	DATA RUN	DRUN	This input informs the WD1010-05/08 when a field of one's or zeroes have been detected.
27	STEP PULSE	STEP	This output generates a pulse for stepping the drive motor.
26	DIRECTION	DIR	This output determines the direction of the stepping motor.

PIN DESCRIPTION (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
28	DRIVE READY	DRDY	This input must be at a logic high in order for commands to execute.
30	WRITE FAULT	WF	An error input to the WD1010-05/08 which indicates a fault condition at the drive.
31	TRACK 000	TK000	An input to the WD1010-05/08 which indicates positioning over track 000.
29	INDEX PULSE	INDEX	A rising edge on this input informs the WD1010-05/08 when the index hole has been encountered.
33	REDUCED WRITE CURRENT	RWC	This output can be programmed to reduce write current on a selected starting cylinder.
32	SEEK COMPLETE	SC	A rising edge on this input informs the WD1010-05/08 when head settling time has expired.

ARCHITECTURE

The WD1010-05/08 Winchester Disk Controller provides the necessary link between an 8-bit, parallel processor and a Winchester disk drive. The WD1010-05/08 may be programmed to either automatically retry errors, or to terminate the command. The internal architecture of the WD1010-05/08 is shown in Figure 1. Its major functional blocks are:

PLA Controller
The PLA interprets commands and provides all control functions. It is synchronized with WCLK.

Magnitude Comparator
A 10 bit magnitude comparator is used for calculation of drive step, direction, present and desired cylinder position.

CRC Logic
Generates and checks the cyclic redundancy check characters appended to the ID and data fields. The polynomial is X16 + X12 + X5 + 1.

MFM Encode/Decode
Encodes and decodes MFM data to be written/read from the drive. The MFM encoder operates from

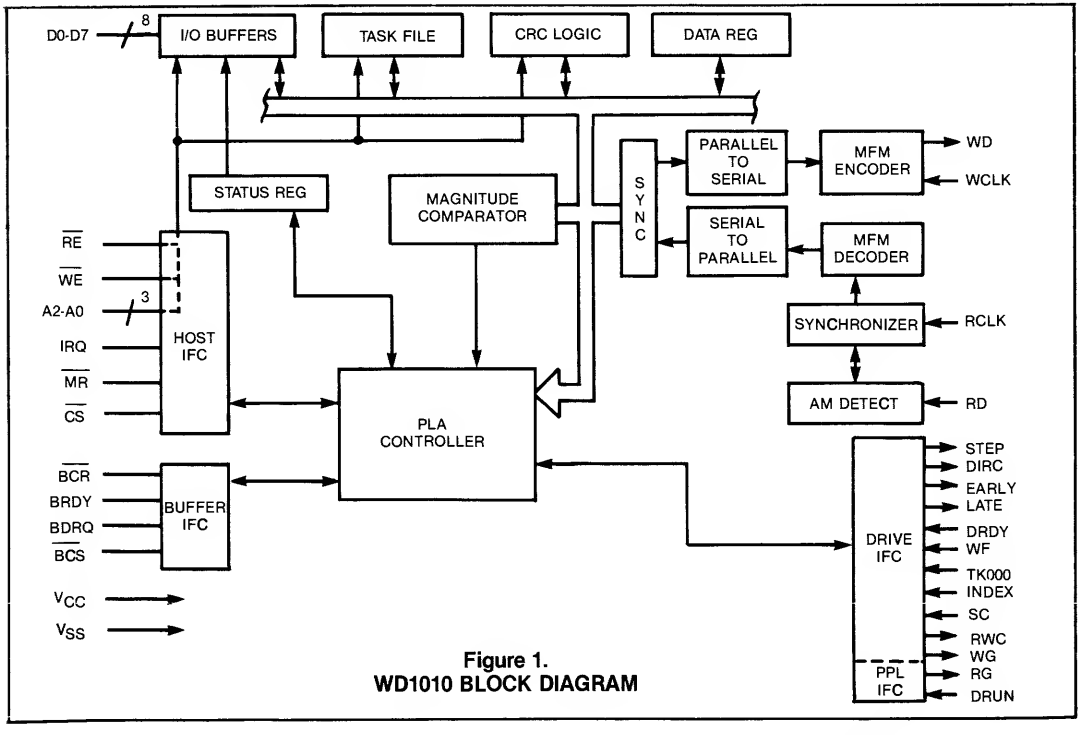


Figure 1.
WD1010 BLOCK DIAGRAM

WCLK; a clock having a frequency equivalent to the bit rate. The MFM decode operates from RCLK; a bit rate clock generated from the external data separator. RCLK and WCLK need not be synchronized.

AM Detect
The address mark detector checks the incoming data stream for a unique missing clock pattern (Data = H'A1', Clock = H'0A') used in each ID and data field.

Host/Buffer IFC
This logic contains all of the necessary circuitry to communicate with the 8-bit host processor.

Drive IFC
This logic controls and monitors all lines from the drive, with the exception of read and write data.

DRIVE INTERFACE

The drive side of the WD1010-05/08 controller requires three sections of external logic. These are buffers/receivers, data separator, and write precompensation. Figure 2 illustrates a drive side interface.

The buffer/receivers condition the control lines to be driven down the cable to the drive. The control lines are typically single-ended, resistor terminated TTL levels. The data lines to and from the drive also require buffering, but are differential RS-422 levels. The interface specification to the drive can be found in the manufacturers' OEM manual. The WD1010-05/08 supplies TTL compatible signals, and will interface to most buffer/driver devices.

The data recovery circuits consist of a phase-lock loop data separator and associated components. The WD1010-05/08 interacts with the data separator through the DATA RUN (DRUN) and Read Gate (RG) signals. The block diagram of the data separator circuit is shown in Figure 3. Read data from the drive is presented to the RD input of the WD1010-05/08, the reference multiplexor, and a retriggerable one shot. The read gate (Pin 38) output will be low when the WD1010-05/08 is not inspecting data. The PLL at this time should remain locked to the reference clock.

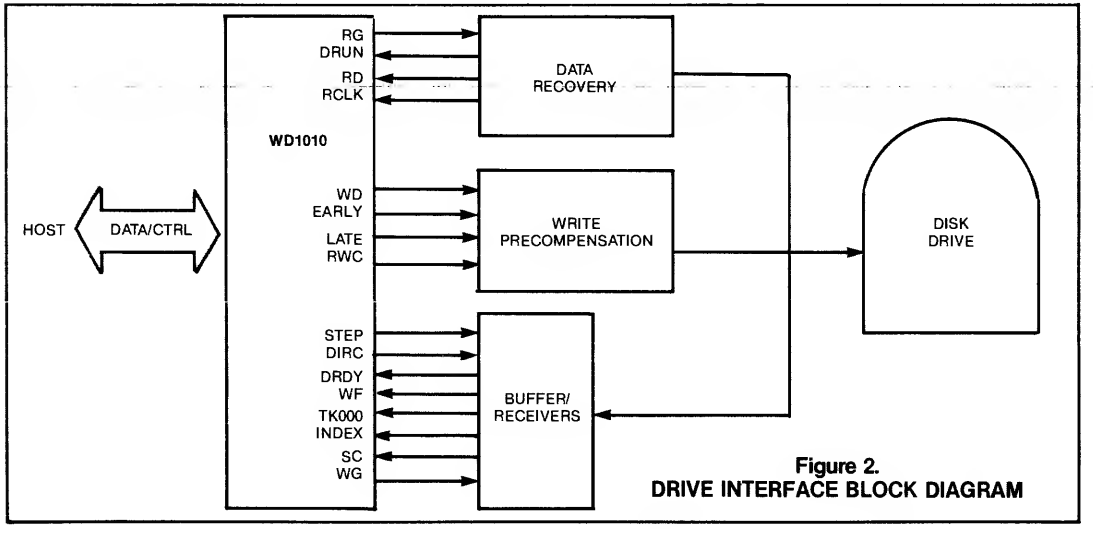


Figure 2.
DRIVE INTERFACE BLOCK DIAGRAM

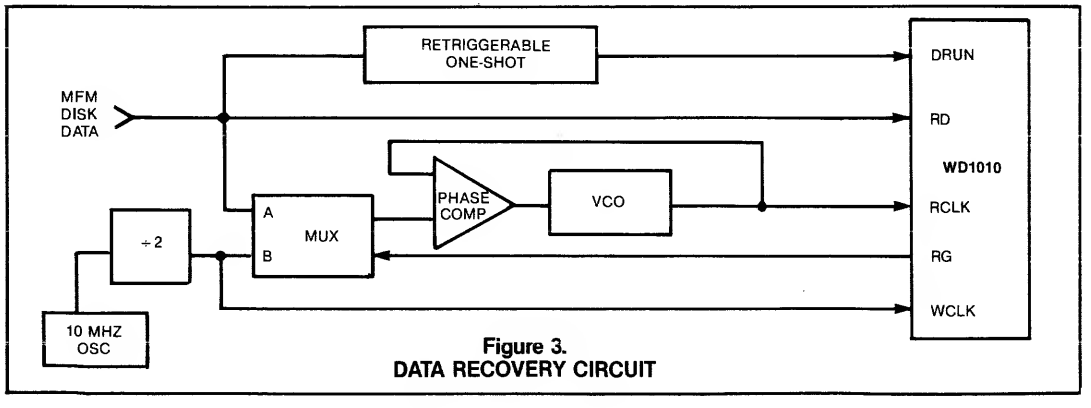


Figure 3.
DATA RECOVERY CIRCUIT

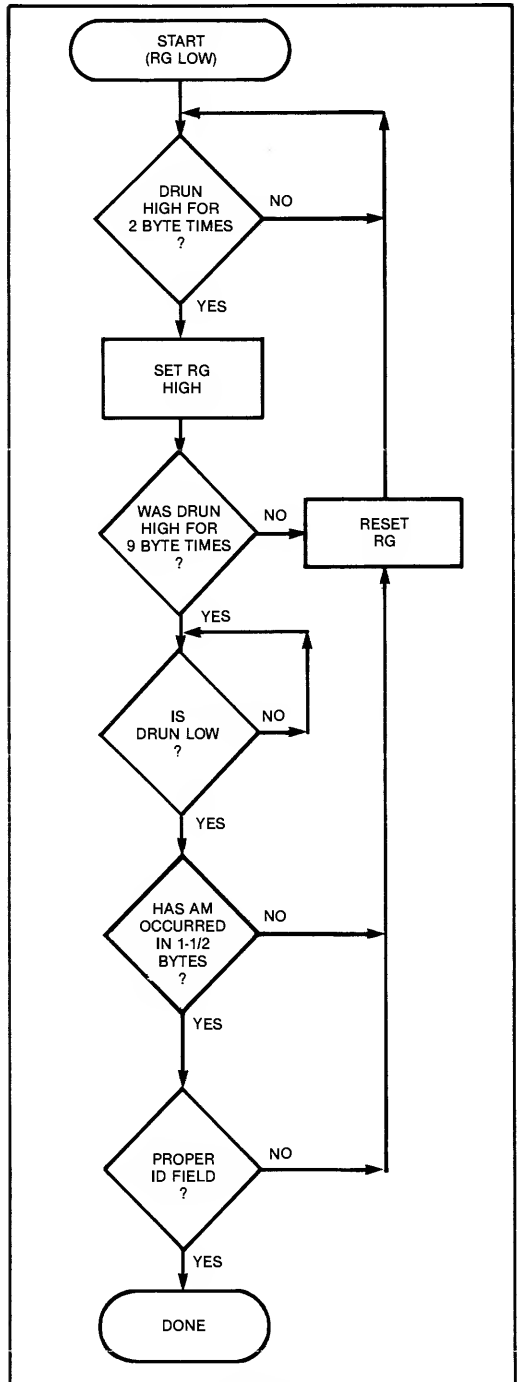


Figure 4.
PLL CONTROL SEQUENCE

When any Read/Write command is initiated and a search for address marks begins, the DRUN input is examined. The DRUN one-shot is set for slightly greater than one bit time, allowing it to retrigger constantly on a field of ones and zeros. An internal counter times out to see that DRUN is high for 16 bits (2 byte times). Read gate is set by the WD1010-05/08, switching the data separator to lock onto the incoming data stream. If DRUN falls prior to 72 bit times RG is lowered and the process is repeated. Read gate will remain active high until a non-zero, non-address mark byte is detected. It then will lower read gate for 2 byte times (to allow the PLL to lock back on the reference clock) and start the DRUN search over again. If an address mark is detected, read gate will be held high and the command will continue searching for the proper ID field. This sequence is shown in the flow chart of Figure 4.

The write precompensation logic is controlled by the signals Reduce Write Current (RWC), $\overline{\text{Early}}$ and $\overline{\text{Late}}$. The cylinder in which the RWC line becomes active is controlled by a register in the Task File. It can be used to turn on the precomp circuitry on a predetermined cylinder. If the write precomp register value is ff, then RWC will always be low.

The signals $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are used to tell the precomp how much delay is required on the write data pulse about to be sent. The amount of delay is determined extemally through a digital delay line or equivalent circuitry. Since the signal $\overline{\text{Early}}$ occurs after the fact, write data should be delayed one interval when both $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are high; two intervals when $\overline{\text{Late}}$ is low; and no delay when $\overline{\text{Early}}$ is low. An interval, for example, is 12-15 ns. on the ST506. $\overline{\text{Early}}$ or $\overline{\text{Late}}$ will be active slightly ahead of the write data pulse; $\overline{\text{Early}}$ and $\overline{\text{Late}}$ will never be low at the same time. Regardless of the contents of the RWC register, $\overline{\text{Early}}$ and $\overline{\text{Late}}$ will always be active.

Examples for all three of the above circuits can be found in the WD1010 Application Note.

HOST INTERFACE

The primary interface between the host processor and the WD1010-05/08 is through an 8-bit bidirectional bus. This bus is used to transmit/receive data to both the WD1010-05/08 and a sector buffer. The sector buffer is constructed with either FIFO memory or static RAM and a counter. Since the WD1010-05/08 will make the bus active when accessing the sector buffer, a transceiver must be used to isolate the host during this time. Figure 5 shows a typical connection to a sector buffer implemented with RAM memory. Whenever the WD1010-05/08 is not using the sector buffer, the Buffer Chip Select ($\overline{\text{BCS}}$) is high (disabled). This allows the host to access the WD1010's Task File, and to set up parameters prior to issuing a command. It also allows the host to access the RAM buffer. A decoder is used to generate a chip select when A_0-A_2 are '000'; an unused address in the WD1010-05/08. A binary counter is enabled when-

ever $\overline{RE}$ or $\overline{WE}$ goes active and incremented on the trailing edge of the chip select. This allows the host to access sequential bytes within the RAM. The decoder also generates another chip select when A_0-$A_2 \neq$ '000'; allowing access to the WD1010-05/08's internal registers while keeping the RAM tri-stated.

During write sector commands, the processor sets up data in the Task File and issues the command. The WD1010 then generates a status to inform the host it may load the buffer with the data to be written. When the counter reaches its maximum count, the Buffer Ready (BRDY) signal is made active (by the "carry" out of the counter), informing the WD1010-05/08 that the buffer is full. (BRDY is a rising edge activated signal.) The Buffer Chip Select ($\overline{BCS}$) is then made active, disconnecting the host through the transceivers, and the $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1010-05/08 to allow it access to the buffer. When the WD1010-05/08 is done using the buffer, it disables $\overline{BCS}$ which again allows host access to this local bus. The read sector commands operate in a similar matter, except the buffer is loaded by the WD1010-05/08 instead of the host.

Another control signal called Buffer Data Request (BDRQ; not used in Figure 5) is a DMA signal that can inform a direct memory access controller when the WD1010-05/08 is requesting data. For further explanation, refer to the description of the individual commands and the A.C. Timing Specifications. In a read command, interrupts are generated at the termination of a command; an interrupt may be specified to occur either at the end of the command or when BDRQ is activated. The interrupt line (INTRQ) is cleared either by reading the status register or by writing a new command in the command register.

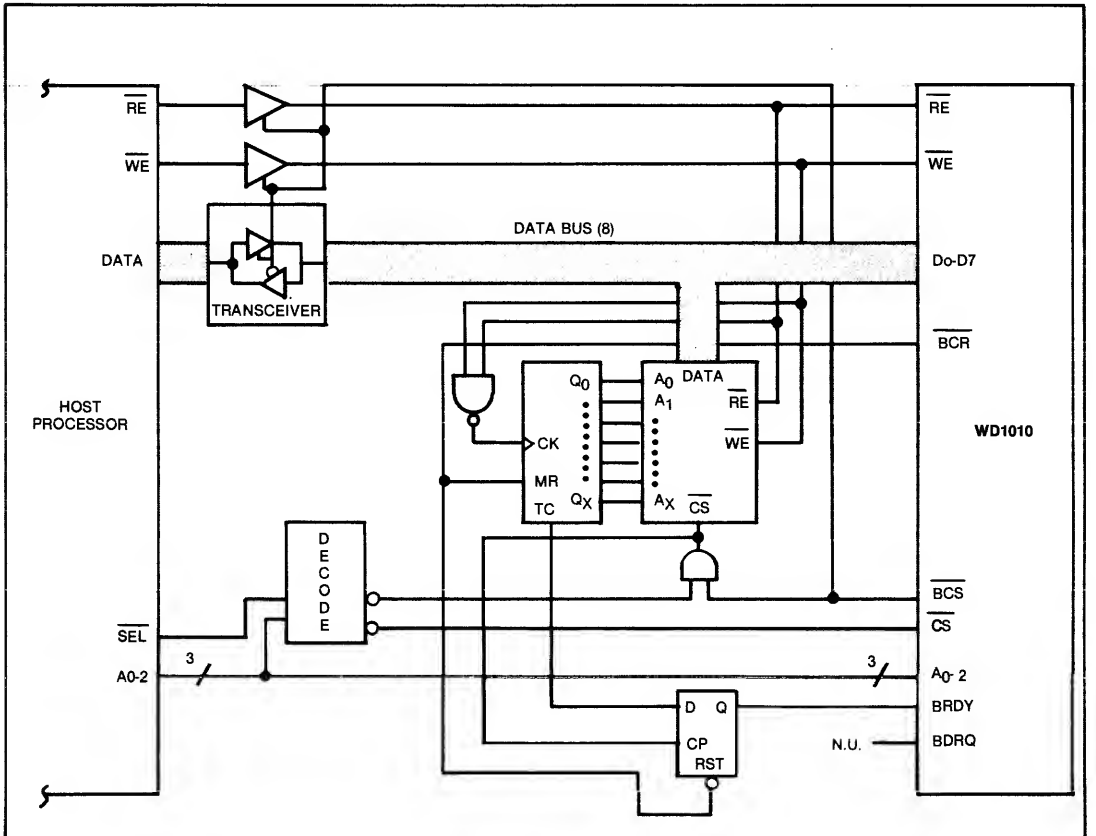


Figure 5.
HOST INTERFACE

TASK FILE

The Task File is a bank of registers used to hold parameter information pertaining to each command. These registers and their addreses are:

A_2	A_1	A_0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE: Registers are **not** cleared by master reset ($\overline{MR}$).

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC	—	ID	—	AC	TK	DM

Bit 7 — Bad Block Detect
This bit is set when an ID field has been encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 — CRC Data Field
This bit is set when a data field CRC error has occurred or the Data Address Mark has not been found. The sector buffer may still be read but will contain errors.

Bit 5 — Reserved
Not used; forced to a zero.

Bit 4 — ID Not Found
This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk, or if an ID field CRC error has occurred.

Bit 3 — Reserved
Not used; forced to a zero.

Bit 2 — Aborted Command
This bit is set if a command was issued while the DRDY (Pin 28) line is low or the WF (30) line is low. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 — TK000 Error
This bit is set only by the restore command. It indictes that the TK000 (Pin 31) line has not gone active after the issuance of 1024 stepping pulses.

Bit 0 — Data Address Mark Not Found
This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.

WRITE PRECOMP CYLINDER

This register is used to define the cylinder number where the RWC (Pin 33) line is asserted:

7	6	5	4	3	2	1	0
CYLINDER NUMBER ÷ 4							

The value (0-255) loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus, a value of H'01' will cause RWC to activate on cylinder 4; H'02' on cylinder 8, and so on. Switching points are then 0, 4, 8, . . . The RWC will be asserted when the present cylinder is equal to a greater than the value in this register. For example, the ST506 requires precomp on cylinder 128 (H'80') and above. Therefore, the write precomp cylinder register should be loaded with 32 (H'20').

A value of H'ff' will always cause RWC to be low, no matter what the cylinder number values are.

SECTOR COUNT

This register holds the number of sectors that are needed to be transferred to the buffer:

7	6	5	4	3	2	1	0
# OF SECTORS							

This register is used during a multiple sector R/W command. The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

This register holds the sector number of a desired sector:

7	6	5	4	3	2	1	0
SECTOR NUMBER							

During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from 0 to 255.

CYLINDER NUMBER LOW

This register holds the least significant 8 bits of the desired cylinder number:

7	6	5	4	3	2	1	0
LS BYTE OF CYLINDER NUMBER							

It is used in conjunction with the cylinder number high register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH

This register defines the two most significant bits of the cylinder number desired:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	(9)	(8)

Internal to the WD1010-05/08, is another pair of registers that hold the actual position number where the R/W heads are located. The cylinder number high and low registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WD1010-05/08 automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a Restore.

SDH BYTE

This register contains the desired sector size, drive number, and head number parameters. The format is:

7	6	5	4	3	2	1	0
EXT	SIZE		DRIVE		HEAD		

6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

Both head number and sector size is compared against the disks' ID field. Head select and drive select lines are not available as outputs from the WD1010-05/08, and must be generated externally. Figure 6 shows the logic to implement these select lines.

Bit 7, the extension bit, is used to extend the data field by seven bytes when using ECC codes. CRC is not appended to the end of the data field when EXT = 1; the data field becomes "sector size + 7" bytes long. CRC is checked on the ID field regardless of the state of the extension bit. Note that the sector size bits are written to the ID during a formatting command. The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written but does have bad block mark written. The format is:

BAD BLOCK	SIZE		0	0	HEAD #		
7	6	5	4	3	2	1	0

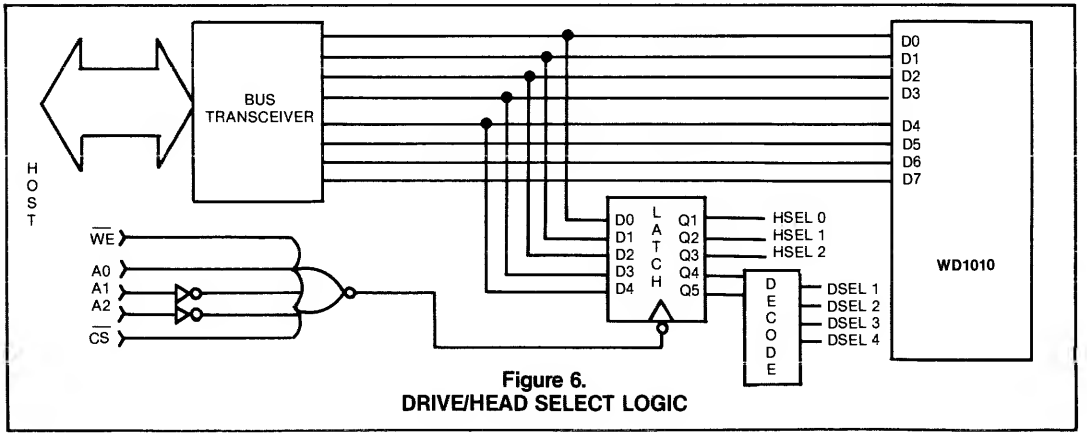


Figure 6.
DRIVE/HEAD SELECT LOGIC

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the WD1010 as well as reporting status from the drive control lines. The format is:

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	—	CIP	ERR

Bit 7 — Busy
This bit is set whenever the WD1010-05/08 is accessing the disk. Commands should not be loaded into the command register while busy is set. Busy is made active when a command is written into the WD1010-05/08 and is deactivated at the end of all commands except the read sector. While executing a read sector command, busy is deactivated after the sector buffer has been filled. When the BUSY bit is set, no other bits in either the status or other registers are valid.

Bit 6 — Ready
This pin normally reflects the state of the DRDY (Pin 28) line. The state of this pin is latched after an 'aborted command' error

Bit 5 — Write Fault
This bit reflects the state of the WF (Pin 30) line. Whenever the WF pin goes high, an interrupt will be generated. The state of this pin latched after an 'aborted command' error.

Bit 4 — Seek Complete
This bit reflects the state of the SC (Pin 32) line. Certain commands will pause until seek complete is true. The state of this pin is latched after 'aborted command' error.

Bit 3 — Data Request
This bit reflects the state of the BDRQ (Pin 36) line. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command. DRQ/BDRQ remains high until BRDY is sensed, indicating the operation is completed. The BDRQ signal can be used in DMA interfacing, while the DRQ bit can be used for programmed I/O transfers.

Bit 2 — Reserved
Not used. This bit is always forced to a zero.

Bit 1 — Command in Progress
When this bit is set, a command is being executed and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host. Only the status register may be read. If other registers are read, the status register contents are returned.

Bit 0 — Error
This bit is set whenever any bits in the error register are set. It is the logical 'or' of the error register and may be used by the host to quickly check successful completion of a command. This bit is reset when a new command is written into the command register.

COMMAND REGISTER

This write-only register is loaded with desired command:

7	6	5	4	3	2	1	0
COMMAND							

The commands begins to execute immediately upon loading. This register should not be loaded while the Busy or CIP bits are set in the status register. The INTRQ (Pin 3) line, if set, will be cleared by a write to the command register.

INSTRUCTION SET

The WD1010 will execute six commands. Prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

COMMAND SUMMARY

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R_3	R_2	R_1	R_0
SEEK	0	1	1	1	R_3	R_2	R_1	R_0
READ SECTOR	0	0	1	0	I	M	0	T
WRITE SECTOR	0	0	1	1	0	M	0	T
SCAN ID	0	1	0	0	0	0	0	T
WRITE FORMAT	0	1	0	1	0	0	0	0

R_3-R_0 Rate Field

For 5 MHz WCLK:
R_3-R_0 = 0000 — ≈35 μs.
0001 — .5 ms.
0010 — 1.0 ms.
0011 — 1.5 ms.
0100 — 2.0 ms.
0101 — 2.5 ms.
0110 — 3.0 ms.
0111 — 3.5 ms.
1000 — 4.0 ms.
1001 — 4.5 ms.
1010 — 5.0 ms.
1011 — 5.5 ms.
1100 — 6.0 ms.
1101 — 6.5 ms.
1110 — 7.0 ms.
1111 — 7.5 ms.

Bit 0, ("T") Read Sector, Write Sector Commands

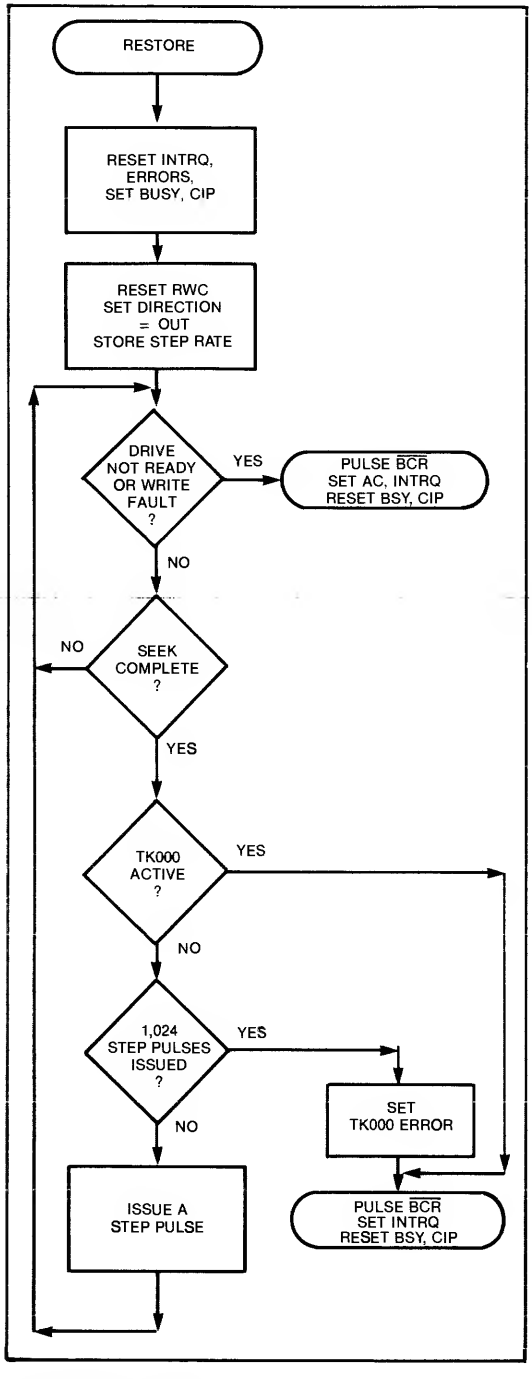
T = 0 Enable retries
T = 1 Disable retries

M = Multiple Sector Flag

M = 0 Transfer 1 sector
M = 1 Transfer multiple sectors

I = Interrupt Enable

I = 0, Interrupt at BDRQ time
I = 1, Interrupt at end of command



RESTORE COMMAND

The restore command is usually used on a power-up condition. The actual stepping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1010-05/08 waits for a rising edge on the seek complete line before issuing the next pulse. If 8 index pulses are received without a rising edge of seek complete, the WD1010 will switch to sensing the level of the SC line. If after 1,024 stepping pulses, the TK000 line does not go active, the WD1010-05/08 will set the TK000 error bit in the error register and terminate with an INTRQ. An interrupt will also occur if the write fault goes active or the DRDY goes inactive during execution.

The rate field specified (R_3-R_0) is stored in an internal register for future use in commands with implied seeks.

SEEK COMMAND

Since all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The actual step rate used is taken from the rate field, which is also stored in an internal register for future use. If DRDY goes inactive or WF goes active, the command is terminated and an INTRQ is generated.

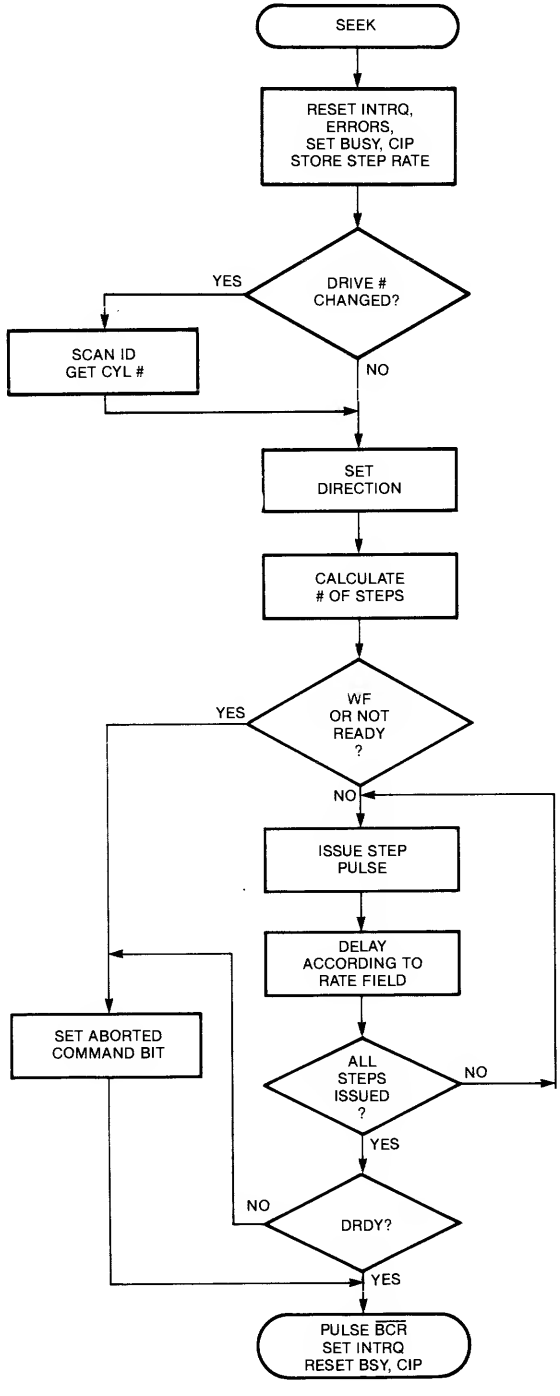
The direction and number of step pulses needed are calculated by comparing the contents of the cylinder register high/low to the cylinder position number stored internally. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. Seek complete is not checked at the beginning or end of the command.

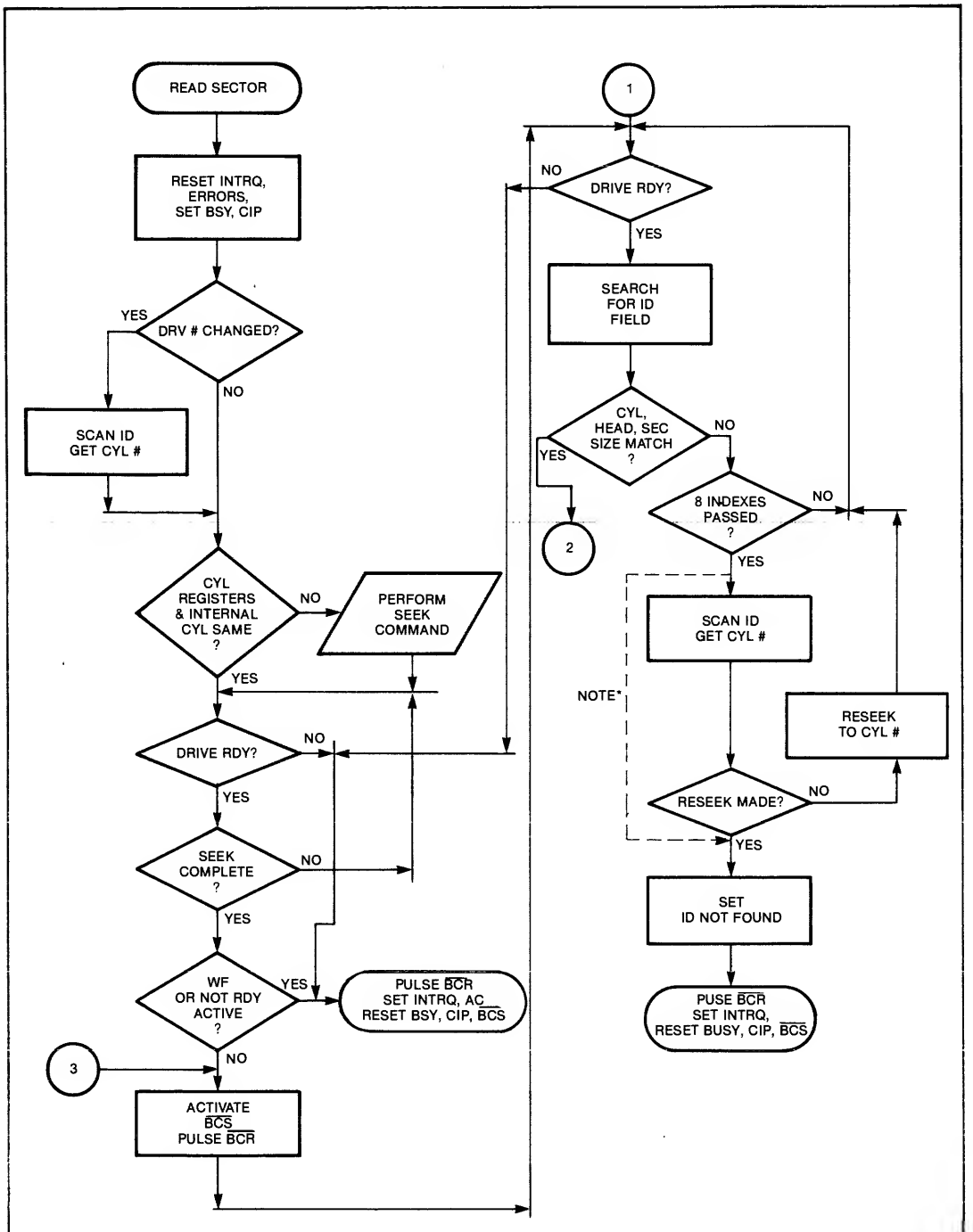
If an implied seek was performed, the WD1010-05/08 will search until a rising edge of Seek Complete is received.

READ SECTOR

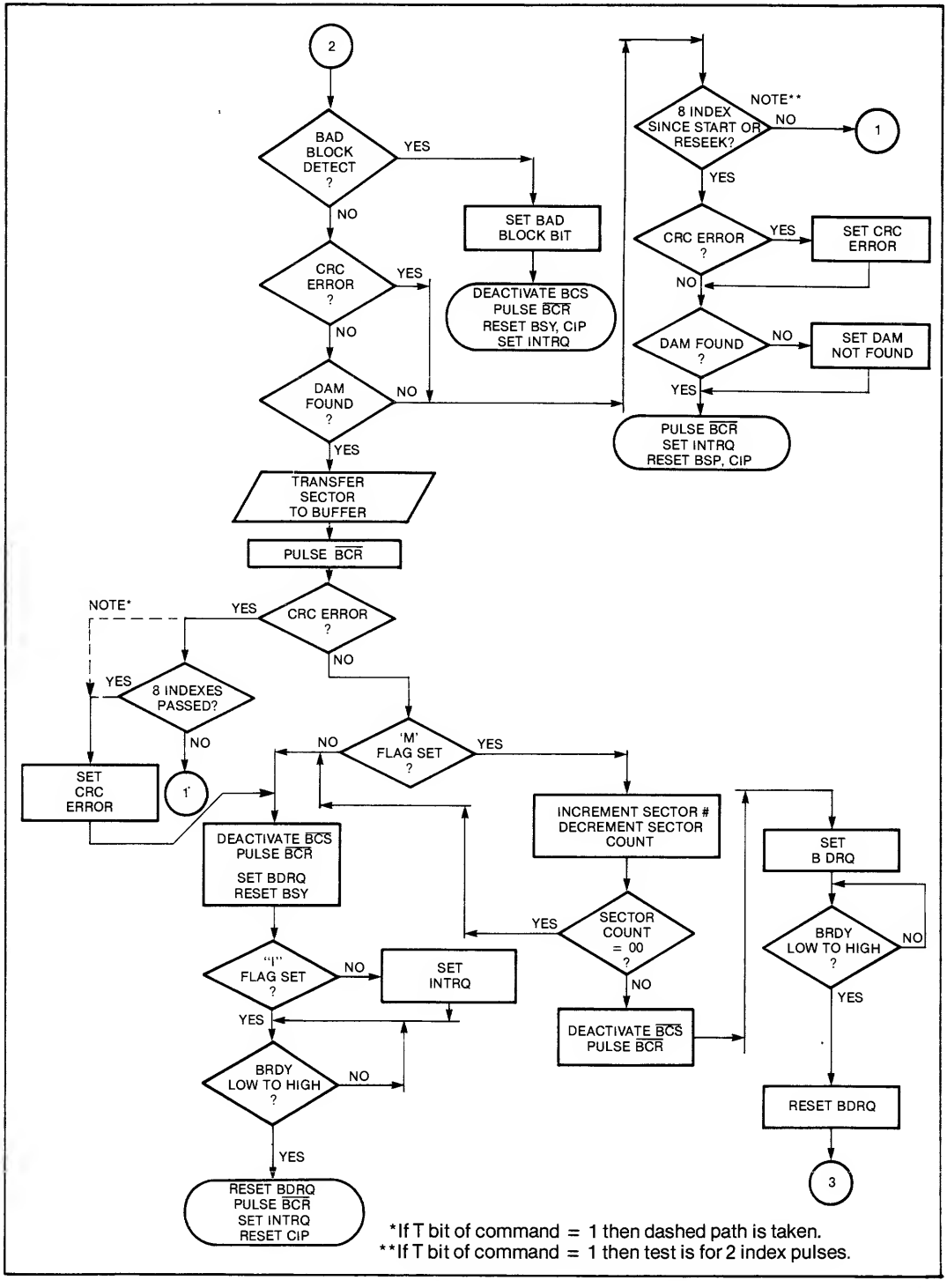
The read sector command is used to transfer one or more sectors of data to the disk. Upon receipt of this command, the WD1010-05/08 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and a seek takes place. If an implied seek was performed, the WD1010-05/08 will search until a rising edge of seek complete is received. Write Fault and DRDY lines are checked throughout the command.

After seek complete is found to be true (with or without an implied seek), the search for an ID field occurs. The WD1010-05/08 must find an ID with the correct cylinder, head, sector size, and CRC within 8 revolutions if T bit of command is zero, and within 2 revolutions if T = 1; else the appropriate error bits will be set and the command terminated if T = 1. Both the Read and Write sector commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command. If T = 0, an automatic scan ID is performed to obtain cylinder position information and then, if necessary, a seek is performed. The search for the correct ID field is continued for 8 more disk rotations.


SEEK
RESET INTRQ, ERRORS, SET BUSY, CIP STORE STEP RATE
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SET DIRECTION
CALCULATE # OF STEPS
WF OR NOT READY ?
YES
NO
ISSUE STEP PULSE
DELAY ACCORDING TO RATE FIELD
SET ABORTED COMMAND BIT
ALL STEPS ISSUED ?
NO
YES
DRDY?
NO
YES
PULSE BCR SET INTRQ RESET BSY, CIP



*If T bit of command = 1 then dashed path is taken after 2 index pulses.



*If T bit of command = 1 then dashed path is taken.
**If T bit of command = 1 then test is for 2 index pulses.

When the data address mark is found, the WD1010-05/08 is ready to transfer data to the buffer. After the sector data has been transferred, the I flag is checked. If the I flag is 0, the INTRQ is made active coincident with BDRQ, indicating a transfer of data is required by the host. If I = 1, the INTRQ will occur at the end of the command (i.e. after the buffer is unloaded by the host).

An optional M flag may be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1010-05/08 decrements the sector count register and increments the sector number register. The next logical sector will be transferred, regardless of the interleave. Sectors are numbered at format time by a byte in the ID field.

For the WD1010 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. The sector transfers will continue until the sector count register equals zero or BRDY goes inactive. If the sector count register is non-zero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the next sector in this multiple sector read command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(5)	1010:	Sets BDRQ = 1; sets DRQ flag.
(6)	1010:	If I bit = 1 then (9).
(7)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$).
(8)	1010:	Waits for BDRY then sets INTRQ = 1; End.
(9)	1010:	Sets INTRQ = 1.
(10)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$); End.

When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; set $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Decrements sector count register; increments sector number register.
(5)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(6)	1010:	Sets BDRQ = 1; DRQ flag = 1.
(7)	Host:	Reads out content of buffer (by $\overline{RE}$ strobes).
(8)	Buffer:	Indicates data has been transferred by asserting BRDY.
(9)	1010:	When BRDY is asserted, go to (11) if sector count = 0.
(10)	1010:	Go to Step (2).
(11)	1010:	Activates INTRQ.

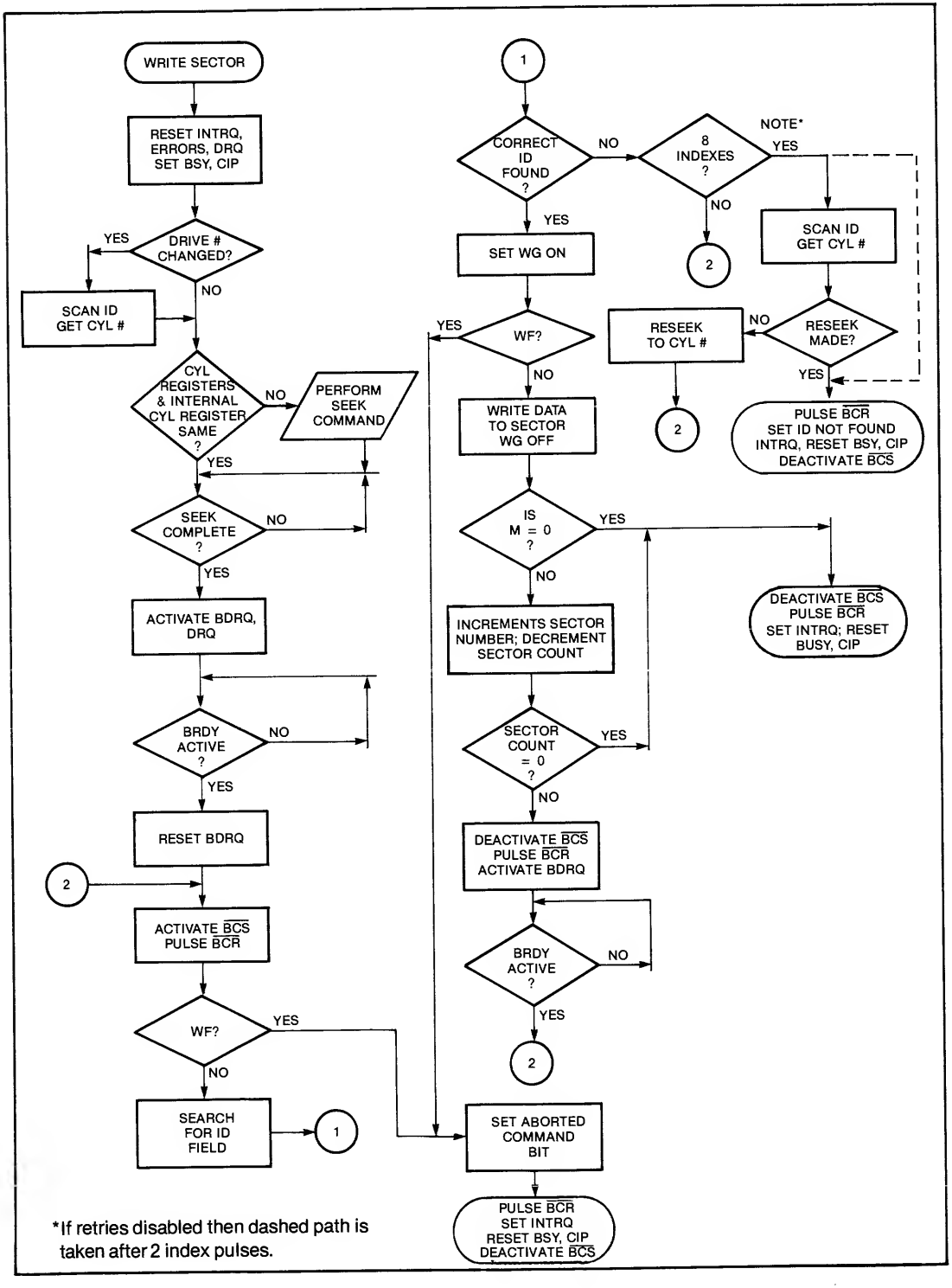
WRITE SECTOR

The write sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1010-05/08 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a seek command takes place. Write fault and DRDY lines are checked throughout the command.

After Seek complete is found to be true (with or without an implied seek), the BDRQ signal is made active and the host proceeds to load the buffer. When the WD1010-05/08 senses the BRDY line going high, the ID field with the specified cylinder, head, and sector size is searched for. Once found, the write gate signal is raised and the data is written to the disk. If retries are disabled and if the ID field cannot be found within 2 revolutions, the ID not found bit is set and the command is terminated.

If retries are enabled, and the ID field cannot be found within 8 revolutions, an automatic scan ID and seek commands are performed. The ID Not Found error bit is set if the ID field is not found after 8 more revolutions.

During a multiple sector write operation (M flag = 1), the sector number is incremented and the sector count register is decremented. If the BRDY line is asserted after the first sector is read out of the buffer, the WD1010-05/08 will continue to read data out of the buffer for the next sector. If BRDY is inactive, the WD1010-05/08 will raise BDRQ and wait for the host


WRITE SECTOR
RESET INTRQ, ERRORS, DRQ SET BSY, CIP
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
CYL REGISTERS & INTERNAL CYL REGISTER SAME ?
NO
PERFORM SEEK COMMAND
YES
SEEK COMPLETE ?
NO
YES
ACTIVATE BDRQ, DRQ
BRDY ACTIVE ?
NO
YES
RESET BDRQ
2
ACTIVATE BCS PULSE BCR
WF?
YES
NO
SEARCH FOR ID FIELD
1
1
CORRECT ID FOUND ?
NO
8 INDEXES ?
NOTE*
YES
NO
2
SCAN ID GET CYL #
RESEEK MADE?
NO
YES
RESEEK TO CYL #
2
PULSE BCR SET ID NOT FOUND INTRQ, RESET BSY, CIP DEACTIVATE BCS
YES
SET WG ON
WF?
YES
NO
WRITE DATA TO SECTOR WG OFF
IS M = 0 ?
YES
NO
DEACTIVATE BCS PULSE BCR SET INTRQ; RESET BUSY, CIP
INCREMENTS SECTOR NUMBER; DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
DEACTIVATE BCS PULSE BCR ACTIVATE BDRQ
BRDY ACTIVE ?
NO
YES
2
SET ABORTED COMMAND BIT
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
*If retries disabled then dashed path is taken after 2 index pulses.

to place more data in the buffer.

In summary then, the write sector operation is as follows:

(1)	Host:	Sets up parameters; issues write sector command.
(2)	1010:	Sets BDRQ = 1, DRQ flag = 1.
(3)	Host:	Loads buffer with data (by $\overline{WE}$ strobes).
(4)	1010:	Waits for BRDY = 1: then reset DRQ, BDRQ.
(5)	1010:	Finds specified ID field, write out sector.
(6)	1010:	If M = 0, then interrupt; End.
(7)	1010:	Increments sector number, decrements sector count.
(8)	1010:	If sector count = 0, then interrupt; End.
(9)	1010:	Go to (2).

SCAN ID

The scan ID command is used to update the head, sector size, sector number and cylinder registers.

The ready and write fault lines are checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, cylinder, and sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, the WD1010-05/08 will retry up to 8 revolutions to find an error-free ID field. There is no implied seek with this command and the buffer is left undisturbed.

FORMAT

The format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 7 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A H'00' is normal; a H'80' indicates a bad block mark for that sector. In the example of Figure 7, sector 04 will get a bad block mark recorded.

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY to tell the WD1010-05/08 to begin formatting the track.

An implied seek is also in effect on this command. As in other commands, if the drive number has changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incompatible format had been used), an IDNF error will result and the Format command will be aborted. This can be avoided by issuing a Restore command before formatting.

The sector count register is used to hold the total number of sectors to be formatted, while the sector number register holds the number of bytes minus 3 to be used for Gap 1 and Gap 3; for instance, if the sector count register value is 2 and the sector number register value is 0, then 2 sectors are written and 3 bytes of H'4E' are written for Gap 1 and Gap 3. The data fields are filled with H'FF,' and CRC is automatically generated and appended. The sector extension bit of the SDH register should not be set. After the last sector is written, H'4E' is filled until index.

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave

	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
:				:				
:				:				
F0	FF	FF	FF	FF	FF	FF	FF	FF

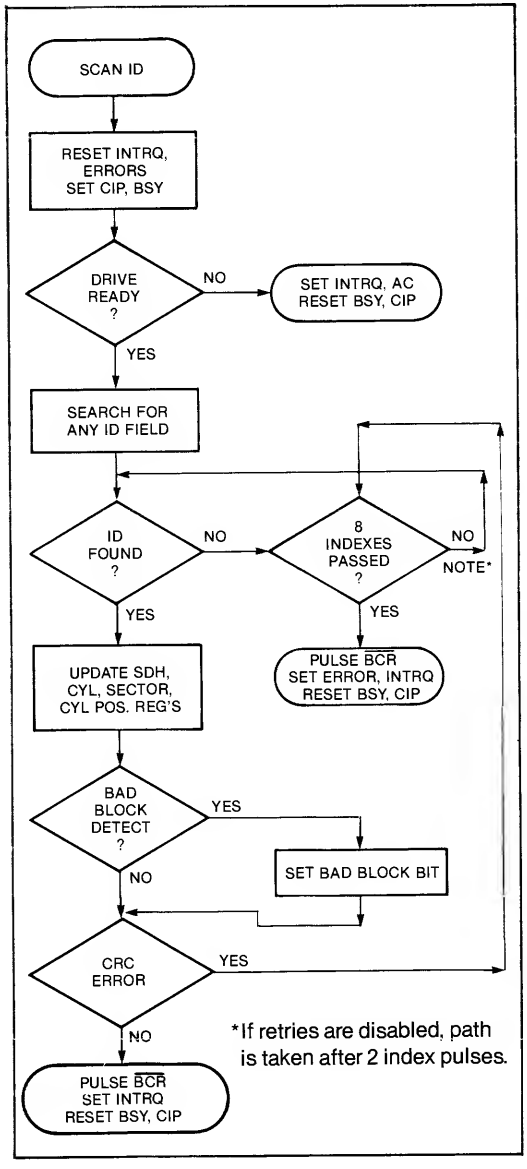
Figure 7.
FORMAT COMMAND BUFFER CONTENTS

factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining the minimum Gap 3 value is:

Gap 3 = 2*M*S + K + E

M = motor speed variation (e.g. .03 for + – 3%)
S = sector length in bytes
K = 25 for interleave factor of 1
K = 0 for any other interleave factor
E = 7 if the sector is to be extended

Like all commands, a write fault or not ready condition will terminate the command. Figure 8 shows the format that the WD1010-05/08 will write on the Disk.



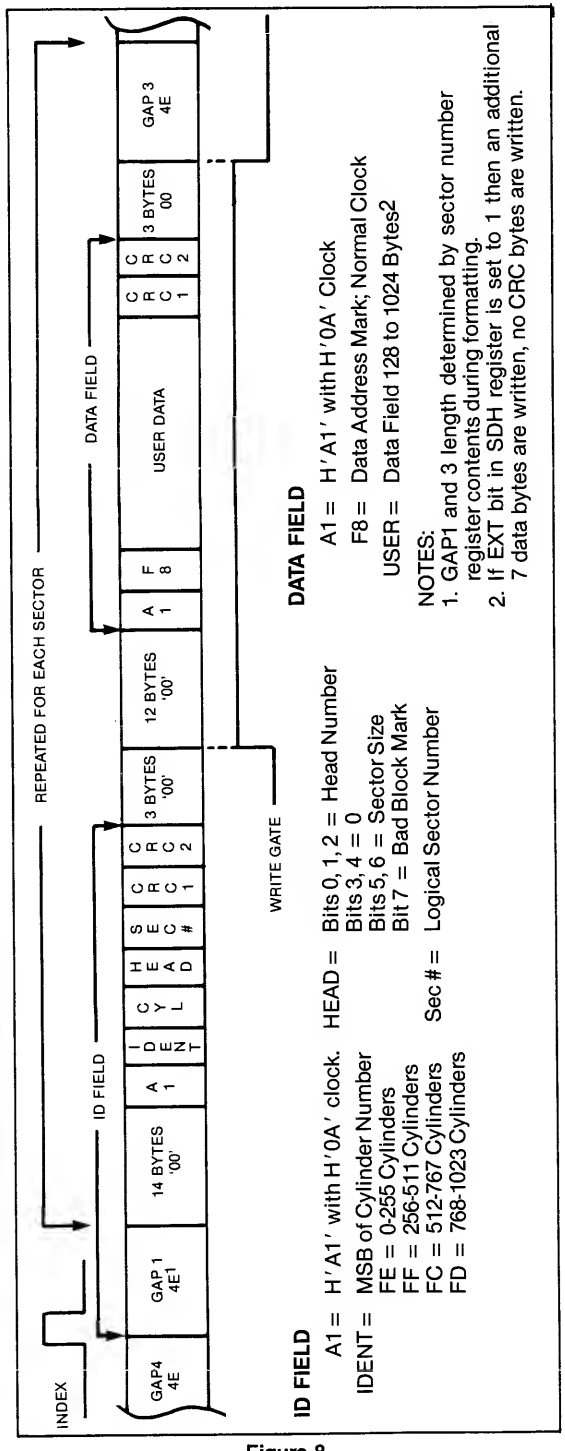
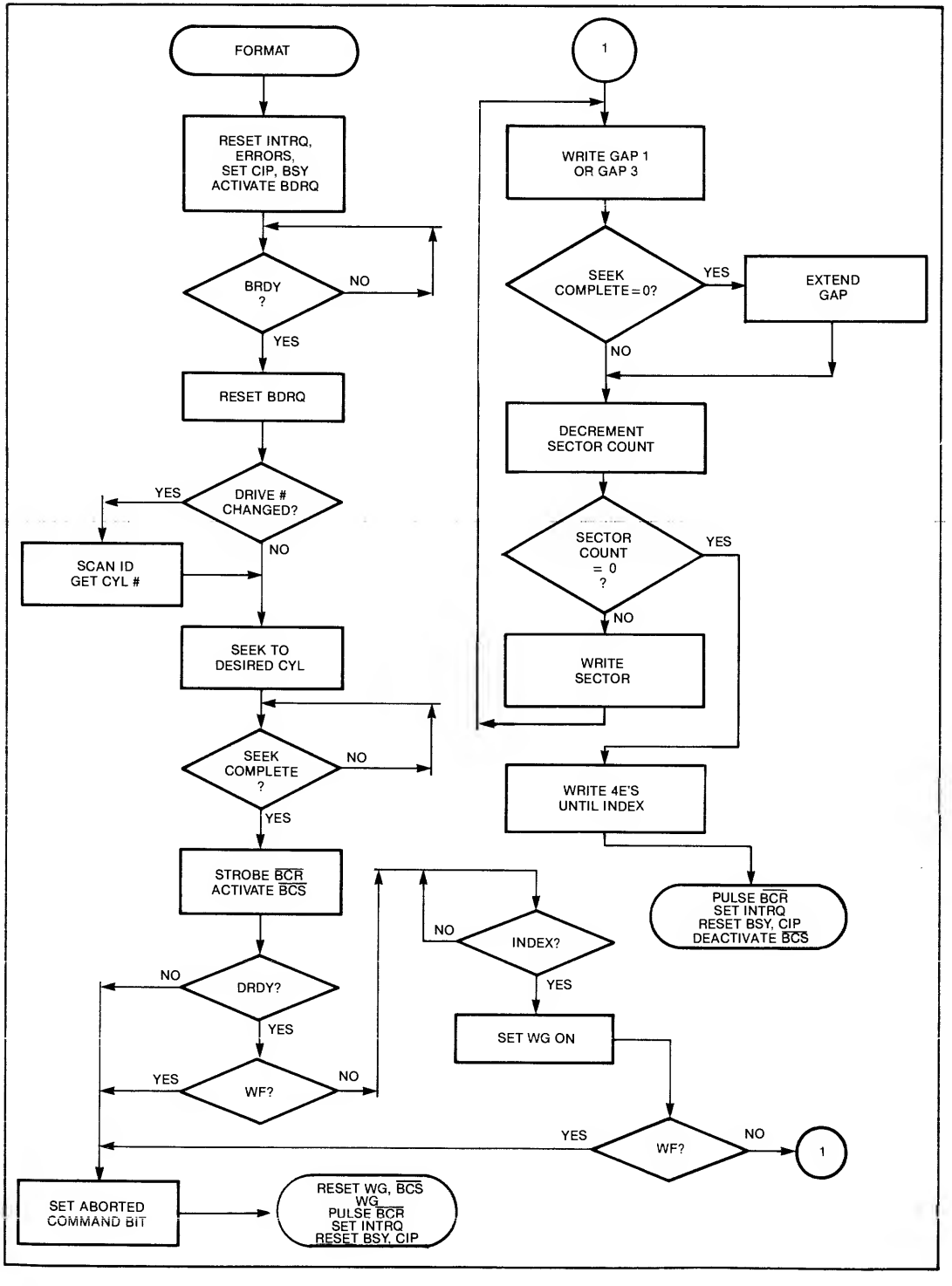


Figure 8. FORMAT


FORMAT
RESET INTRQ, ERRORS, SET CIP, BSY ACTIVATE BDRQ
BRDY ?
NO
YES
RESET BDRQ
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SEEK TO DESIRED CYL
SEEK COMPLETE ?
NO
YES
STROBE BCR ACTIVATE BCS
DRDY?
NO
YES
WF?
YES
NO
SET ABORTED COMMAND BIT
RESET WG, BCS WG PULSE BCR SET INTRQ RESET BSY, CIP
1
WRITE GAP 1 OR GAP 3
SEEK COMPLETE=0?
YES
EXTEND GAP
NO
DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
WRITE SECTOR
WRITE 4E'S UNTIL INDEX
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
INDEX?
NO
YES
SET WG ON
WF?
YES
NO
1

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with
respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Drain)		±10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = −100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
V_{OL}	Output Low Voltage (Pins 21-23)		0.45	V	IO = 4.8 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	For Pins 25, 34, 37, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise Time		30	ns	10% to 90% points

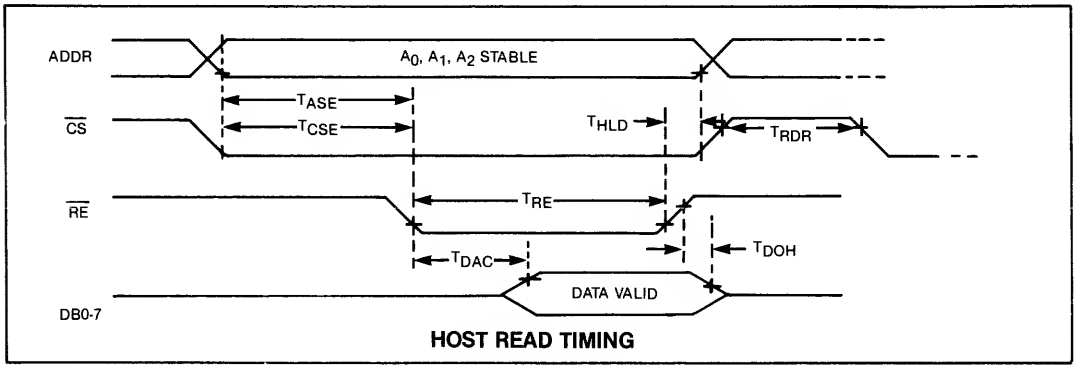
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

HOST READ TIMING WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{ASE}	ADDR Setup to $\overline{RE}$	100		ns	
T_{DAC}	Data Valid from $\overline{RE}$		375	ns	
T_{RE}	Read Enable Pulse Width	.4	10	μs	
T_{DOH}	Data Hold from $\overline{RE}$	20	200	ns	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		ns	
T_{RDR}	Read Recovery Time	300		ns	
T_{CSE}	$\overline{CS}$ Setup To $\overline{RE}$	0		ns	

HOST READ TIMING WD1010-08 WC = 8 MHZ

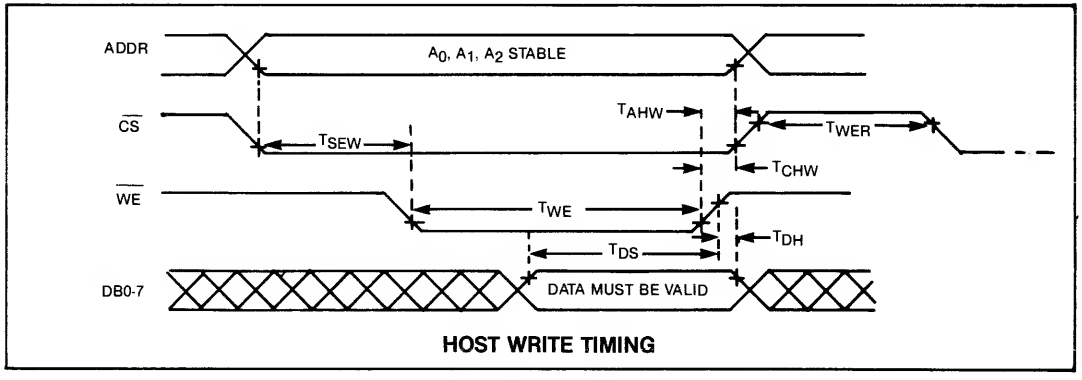
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{ASE}	ADDR Setup to $\overline{RE}$	100		ns	
T_{DAC}	Data Valid from $\overline{RE}$		250	ns	
T_{RE}	Read Enable Pulse Width	.3	10	μs	
T_{DOH}	Data Hold from $\overline{RE}$	20	100	ns	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		ns	
T_{RDR}	Read Recovery Time	300		ns	
T_{CSE}	$\overline{CS}$ Setup To $\overline{RE}$	0		ns	



HOST READ TIMING

HOST WRITE TIMING WD1010-05/08

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SEW}	ADDR, CS Setup to $\overline{WE}$	0	10	μs	
T_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	μs	
T_{WE}	Write Enable Pulse Width	.2	10	μs	
T_{DH}	Data Bus Hold from $\overline{WE}$	10		ns	
T_{AHW}	ADDR Hold from $\overline{WE}$	30		ns	
T_{WER}	Write Recovery Time	1.0		μs	See Note 1
T_{CHW}	$\overline{CS}$ Hold Time	0			



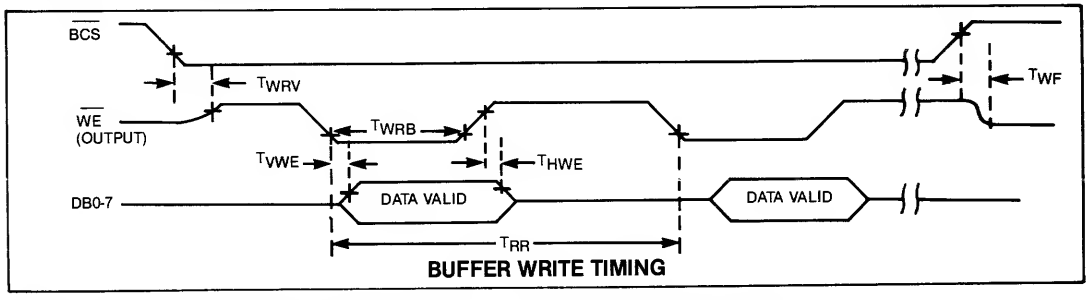
HOST WRITE TIMING

BUFFER WRITE TIMING (READ SECTOR CMD) WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	ns	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{VWE}	Data Valid from $\overline{WE}$			110	ns	
T_{HWE}	Data Hold from $\overline{WE}$	60			ns	
T_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	μs	See Note 2
T_{WF}	$\overline{WE}$ Float from BCS	15		100	ns	C_L = 50 pf

BUFFER WRITE TIMING (READ SECTOR CMD) WD1010-08 WC = 8 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	ns	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	200	250	500	ns	See Note 7
T_{VWE}	Data Valid from $\overline{WE}$			100	ns	
T_{HWE}	Data Hold from $\overline{WE}$	60			ns	
T_{RR}	$\overline{WE}$ Repetition Rate	.75	1.0	1.25	µs	See Note 2
T_{WF}	$\overline{WE}$ Float from BCS	15		100	ns	C_L = 50 pf



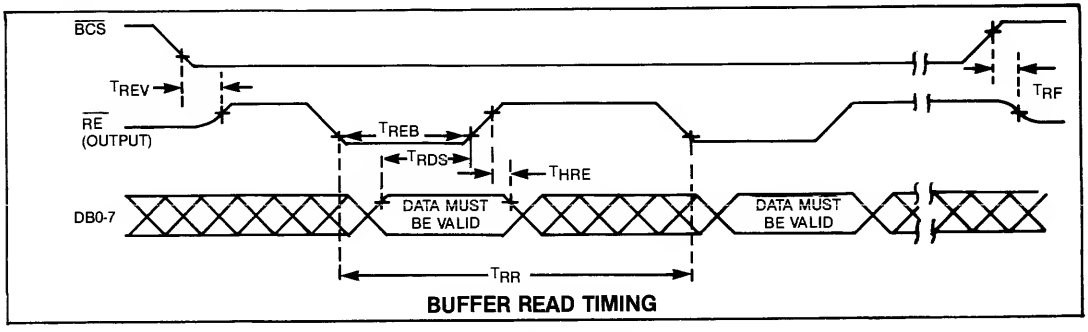
BUFFER WRITE TIMING

BUFFER READ TIMING (WRITE SECTOR CMD) WD1010-05 WC = 5 MHZ

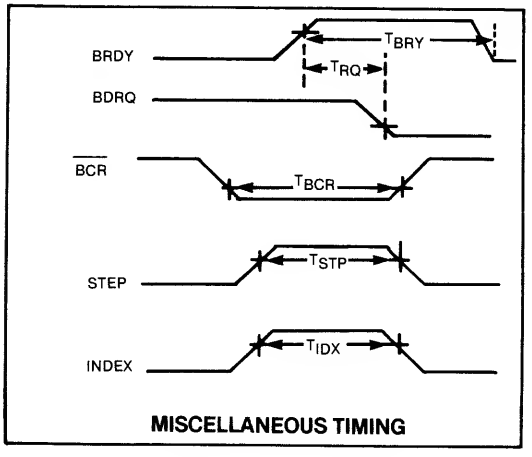
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	ns	C_L = 50 pf
T_{REB}	RE Output Pulse Width	300	400	500	ns	See Note 4
T_{RDS}	Data Setup to $\overline{RE}$	140			ns	
T_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	µs	
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	ns	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			ns	

BUFFER READ TIMING (WRITE SECTOR CMD) WD1010-08 WC = 8 MHZ

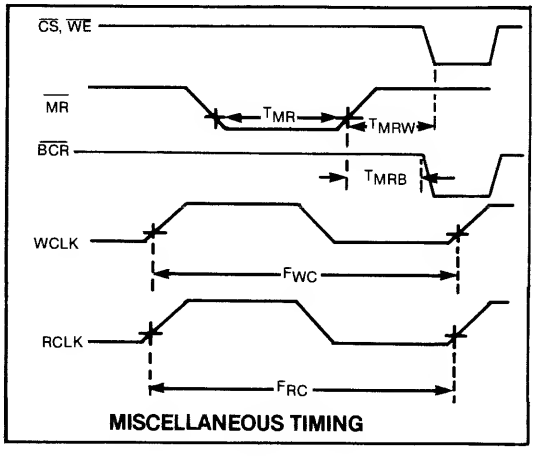
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	ns	C_L = 50 pf
T_{REB}	RE Output Pulse Width	200	250	300	ns	See Note 7
T_{RDS}	Data Setup to RE	100			ns	
T_{RR}	$\overline{RE}$ Repetition Rate	.75	1.0	1.25	µs	
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	ns	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			ns	



BUFFER READ TIMING



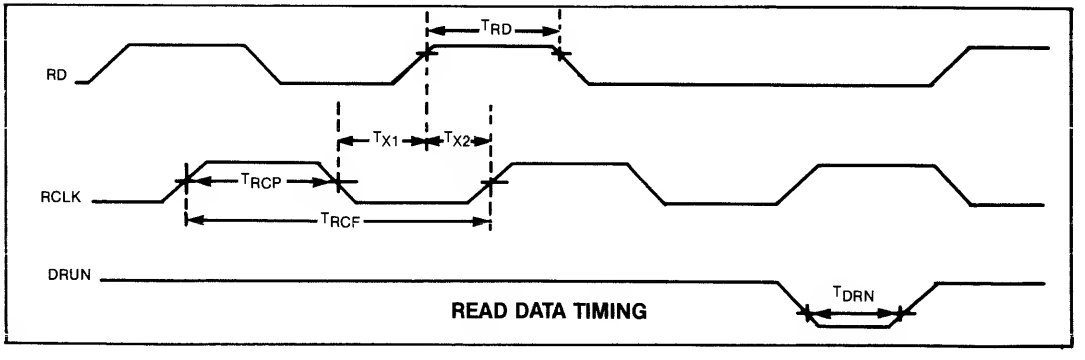
MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RQ}	BDRQ Reset from BRDY	40		200	ns	
T_{BCR}	Buffer Counter Reset Pulse Width	1.4	1.6	1.8	µs	See Note 2
T_{STP}	Step Pulse Width	8.3	8.4	8.7	µs	See Note 2
T_{IDX}	Index Pulse Width	500			ns	
T_{MR}	Master Reset Pulse Width	24			WC	See Note 3
$F_{WC(-05)}$	Write Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle, WD1010-05
$F_{RC(-05)}$	Read Clock Frequency	.25	5.0	5.25	MHz	See Note 6
$F_{WC(-08)}$	Write Clock Frequency	.25	8.0	8.4	MHz	50% Duty Cycle, WD1010-08
$F_{RC(-08)}$	Read Clock Frequency	.25	8.0	8.4	MHz	See Note 6
T_{BRY}	BRDY Pulse Width	800			ns	See Note 5
T_{MRB}	$\overline{MR}$ Trailing To $\overline{BCR}$	1.6	3.2	6.4	µs	See Note 2
T_{MRW}	$\overline{MR}$ Trailing To Host Write	6.4			µs	See Note 2



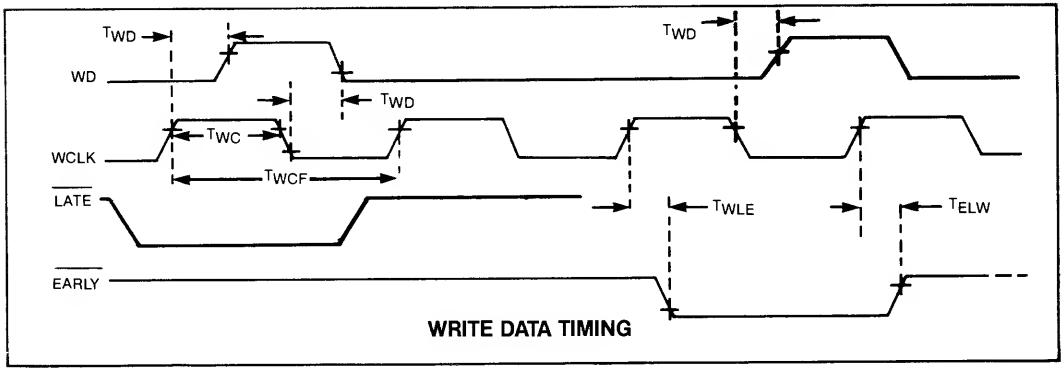
READ DATA TIMING

READ DATA TIMING WD1010-05 WD = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	95		2000	ns	50% Duty Cycle
T_{X1}	RD from RCLK Transition	0		$T_{RCP} \div 2$	ns	
T_{X2}	RD to RCLK Transition	20		$T_{RCP} \div 2$	ns	
T_{RD}	RD Pulse Width	40		T_{RCP}	ns	
T_{DRN}	DRUN Pulse Width	30			ns	
T_{RCF}	RCLK Frequency	.250		5.25	MHZ	See Note 6

READ DATA TIMING WD1010-08 WD = 8 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	60		2000	ns	50% Duty Cycle
T_{X1}	RC Transition to Next Leading RD	0		$T_{RCP} \div 2$	ns	
T_{X2}	Leading RD to Next RC Transition	10		$T_{RCP} \div 2$	ns	
T_{RD}	RD Pulse Width	30		T_{RCP}	ns	
T_{DRN}	DRUN Pulse Width	25			ns	
T_{RCF}	RCLK Frequency	.250		8.4	MHZ	See Note 6



WRITE DATA TIMING

WRITE DATA TIMING WD1010-05 WD = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	ns	
T_{WD}	Prepagation Delay WCLK to WD	10		65	ns	
T_{WLE}	WCLK to Leading Early/Late	10		65	ns	
T_{ELW}	WCLK to Trailing Early/Late	10		65	ns	
T_{WCF}	WCLK Frequency	.250		5.25	MHZ	See Note 6

WRITE DATA TIMING WD1010-08 WD = 8 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	ns	
T_{WD}	Prepagation Delay WCLK to WD	10		45	ns	
T_{WLE}	WCLK to Leading Early/Late	10		45	ns	
T_{ELW}	WCLK to Trailing Early/Late	10		65	ns	
T_{WCF}	WCLK Frequency	.250		8.4	MHZ	See Note 6

NOTES:
1. AC timing measured at $V_{OH} = 2.0V$, $V_{OL} = 0.8V$, $C_L = 50$ pf.
2. Based on WCLK = 5.0 MHz. Multiply timings by .625 for 8 MHz operation.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz).
4. 2 WCLK ± 100 ns.
5. BRDY must be >4 μs or a spurious BDRQ pulse may exist for up to 4 μs after rising edge of BRDY.
6. $T_{RCF} = T_{WCF} \pm 15\%$.
7. 2 WCLK ± 50 ns.

See page 481 for ordering information.

Printed in U.S.A

WD1010 Application Notes

FLEXIBLE CONTROLLER MATES WITH POPULAR WINCHESTER DRIVES

To take advantage of the growing demand for Seagate Technology-type 5¼-in. Winchester disk drives in personal computers, electronic work stations, and small-business systems, designers need an appropriate controller that is inexpensive. In fact, today's designs must implement the control link between a host CPU and a disk drive at far lower cost than the drive itself. That requires a single-chip controller rather than discrete, gate-array-intensive circuits that take up valuable board space in ever smaller computer equipment.

Such a device is now available in the form of an LSI single-chip Winchester controller-formatter. The chip incorporates 80% of the circuitry required for Winchester control, eliminating between 50 and 75 SSI and MSI devices used in earlier designs.

A controller that claims Seagate compatibility must be sufficiently flexible to meet not only the company's original ST506 specifications, but also the various deviations from them. The basic specifications include a data rate of 5.0 Mbits/s and open-collector outputs and differential signal inputs for the separate control and data interface cables. The recording format is modified frequency modulation (MFM), but more importantly, the structure of the format defines both specific address-mark bytes and ID fields. These are fixed specifications, but manufacturers of Seagate-type drives sometimes make other changes. For example, the track density on high-capacity drives may be greater than that in the original ST506 specifications. Also, the number of sectors and bytes per sector on each cylinder can vary according to the application. In each case, a compatible controller must be able to handle the original specifications plus the deviations.

The ST506 interface is a spinoff of the Shugart Associates SA1000 drive, first introduced in 1979. Two important differences between the interfaces are the data rates and a timing-clock differential signal on the SA1000. The latter operates at 4.34 Mbits/s vs 5 Mbits/s for the ST506, but the remaining signals have enough similarity to permit a single controller design to run either an 8-in. SA1000 drive or the 5¼-in. ST506 drive. The advantage of the WD1010 Winchester controller-formatter is that it works with either and with other manufacturers' variations as well.

Operation of the drive begins when a host processor initiates a command after first loading a set of internal task registers called the task file. Information such as cylinder, sector, and head number is written to these registers, which are selected by address lines. The memory-mapped register scheme allows individual accesses to each register. Thus the host need not waste valuable time reading all the registers to obtain a specific parameter.

The WD1010, which comes in a 40-pin DIP, is run by an internal microcontroller — a PLA (programmable logic array) serving as a state machine (Fig. 1). This logic controls the flow of data throughout the chip, recognizes and processes commands, and formats the data.

WRITING AND READING DATA

During a write operation, parallel data is read from the data bus and written to a specific sector. But first the cylinder and sector must be located on the requested disk drive. The WD1010's micro-controller accesses its internal cylinder-position data and compares it with the requested cylinder number. If necessary, a seek is performed automatically to position the head assembly over the desired cylinder.

If the drive requested is changed before a seek command is executed, the WD1010 enables its read logic and searches for an ID field on the currently selected drive. Then it reads the cylinder number from the new ID field and determines whether to seek in or out to find the requested cylinder. This so-called implied seek is a feature of all commands (see "Macro Commands Provide Multiple Options").

After the WD1010 finds an ID field that matches the cylinder, head, sector, sector size and CRC (cyclic redundancy check) value, it writes a field of 0s and a new address mark — later these two fields will be used for synchronization during a read operation. The chip then reads parallel data in from the data bus, serializes it, and converts it into the MFM format. Next, a new CRC value is calculated for the incoming data and is appended to the end of the data field (after the last byte). If the original command specified multiple sectors, the next logical sector must be searched for and the process repeated. After the last sector is written, the WD1010 gives the bus back to the host and waits for the next command.

Although the chip does not generate an error correction signal, an optional command bit can be set to disable cyclic redundancy checks of the data field. The sector is extended by seven bytes to allow the host to write its 56-bit error detection and correction code. Later, during a read operation, these seven bytes are transferred back to the host to permit it to identify a syndrome and correct any errors that were encountered. For systems that require such operations, the WD1014 error detection and correction and

WD1015 buffer controller chips are available.

Reading is similar to writing except that data is sent out on the data bus and written into the sector buffer at the host. MFM data is entered on the RD pin along with a synchronous clock (RCLK) generated from an external data separator (Figure 2).

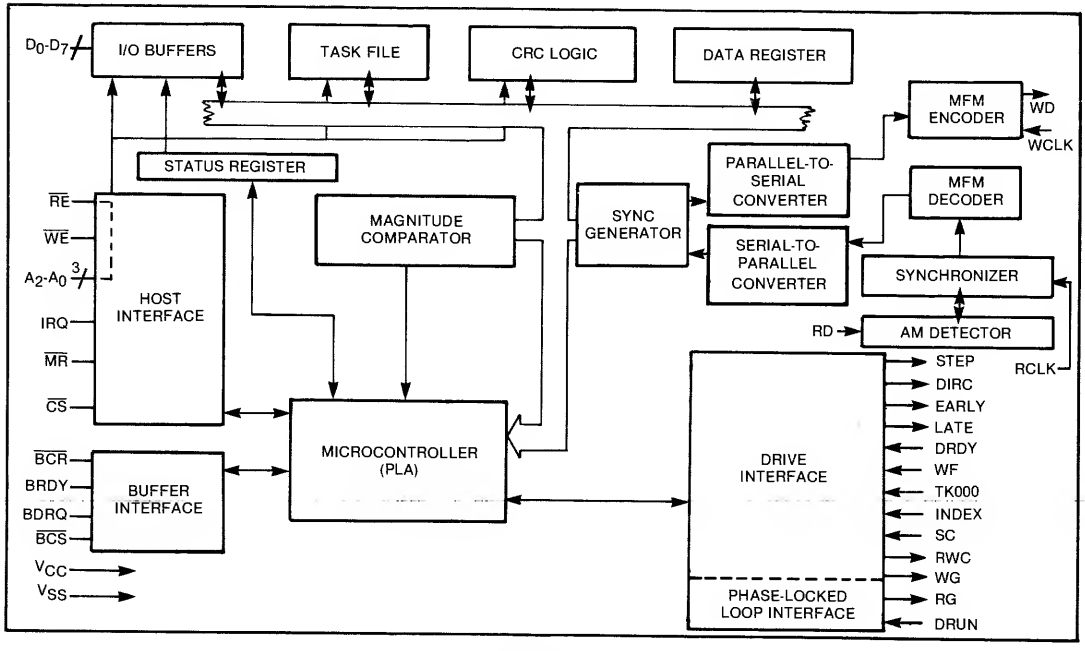


Figure 1.

The architecture of the WD1010 Winchester controller-formatter chip is designed to reduce a host processor's overhead burden. An internal microcontroller (PLA) manages data flow, incoming commands, and formatting.

Since the data rate is relatively high, the data separator must instruct the controller to lock on to the incoming data stream only during a field of 1s and 0s. A Data Run (DRUN) signal to the WD1010 indicates such an occurrence. When DRUN is active, the WD1010 counts off 16 bits — 2 byte times — sets the Read Gate (RG) signal, and starts to search the data stream for an address mark.

IMPLEMENTING THE PRECOMPENSATION ALGORITHM				
ALREADY SENT		SENDING	TO BE SENT	SHIFT REQUIRED
X	1	1	0	Early
X	0	1	1	Late
0	0	0	1	Early
1	0	0	0	Late

NOTE: All other patterns produce no shift.

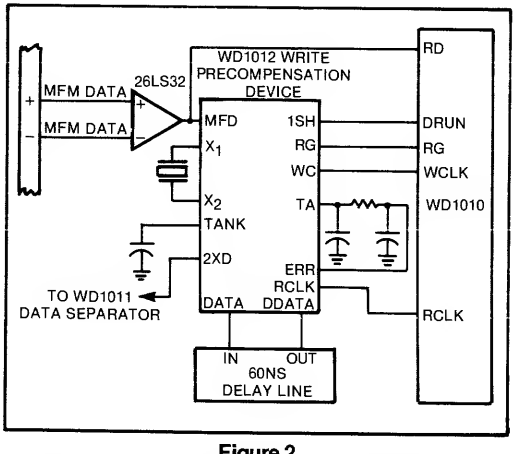


Figure 2.

A separate IC — the WD1012 — performs the data separation for the WD1010. The data separator sends a DRUN signal to the controller when it encounters a data field (1s and 0s).

An address mark is a unique pattern of clock and data bits that does not appear in any place that normal MFM data appears. If an address mark is not detected within nine bytes or if a non-0 pattern is detected within nine bytes, RG is turned off and the search repeated. Since data fields within sectors can contain 0s or all 1s, the DRUN algorithm is also triggered in these cases. But the address mark will not be detected, preventing erroneous data from being transferred.

After the ID field is compared and verified, a search begins for the address mark. Resynchronization occurs and the data is transferred to an internal MFM-to-NRZ converter. Data is then shifted through a double-buffered shift register and placed on the data bus for loading to the buffer. Either the cyclic redundancy code at the end of the data field is checked or the error detection and correction bytes are transferred in parallel to the host, depending on which option is used. Then the host processor can read the data from its local buffer.

Like all magnetic recording media, Winchester disks are not immune to the effects of bit shifts at high recording densities. The WD1010 uses an algorithm that informs external delay circuits when to shift outgoing data. A register within the task file specifies which cylinder receives reduced write current and if precompensation is needed. Typically, both occur on the same cylinder about half way down the disk surface.

The WD1010's precompensation signals are called $\overline{\text{Early}}$ and $\overline{\text{Late}}$. Depending on the bit pattern leaving the device, data will be shifted early, late, or not at all. A WD1011 data separator implements the precompensation delay network (Figure 3).

Since the $\overline{\text{Early}}$ signal and the current data (or clock) bits leaving the WD1010 have already occurred, the WD1011 performs no delay function on $\overline{\text{Early}}$. If both $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are inactive, the WD1011 inserts a 12-ns delay; if only $\overline{\text{Late}}$ is active, it inserts a 24-ns delay. The result is a ± 12-ns shift of the data from its nominal position. An inactive Reduced Write Current (RWC) signal from the WD1010 disables the WD1011. The WD1010 then furnishes precompensation signals independent of current cylinder position.

INTERFACING WITH CABLES AND BUSES

The remaining function on the drive side is to provide sufficient buffers to drive the cables between the chip and the interface connectors. Single-ended open-collector signals are used for the control cable, and differential receiver-drivers are used for the data cable (Figure 4). Each line must have such buffers, since the controller is designed to drive one TTL load on all inputs and outputs.

At a 5-Mbit/s data transfer rate to the host interface, a byte of data must be read every 1.6 μs — in 8-bit parallel form. Few microprocessors can access a port and check status within this period. Consequently, a design objective of the WD1010 is compatibility with a programmed I/O environment, as well as the support of off-line error detection and correction. Moreover, the chip can transfer multiple sectors on one command. To achieve such performance within the constraints of a 40-pin package, the WD1010 relies on a unique approach to the traditional peripheral interface.

Three modes of communication can exist at the host interface: between the host and the WD1010, between the host and the buffer, and between the WD1010 and the buffer. For host-WD1010 commun-

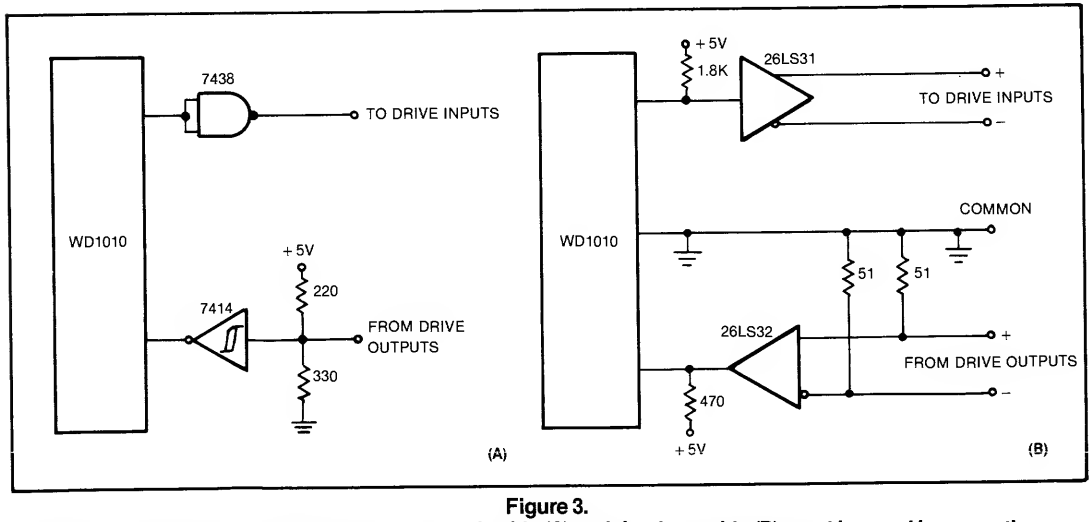


Figure 3.
Buffering circuits from the WD1010 to the control cable (A) and the data cable (B) must be used because the controller has a rather limited drive capability (one TTL load each on inputs and outputs).

ication the chip, like many microprocessors, talks over an 8-bit bidirectional bus, plus Read, Write and chip select lines (Figure 5). Three address lines access registers within the chip.

In host-buffer or WD1010-buffer communications (Figure 6), when the chip reads or writes to the buffer, the Buffer Chip Select ($\overline{BSC}$) line is pulled low. This signal should be used to disconnect the host data

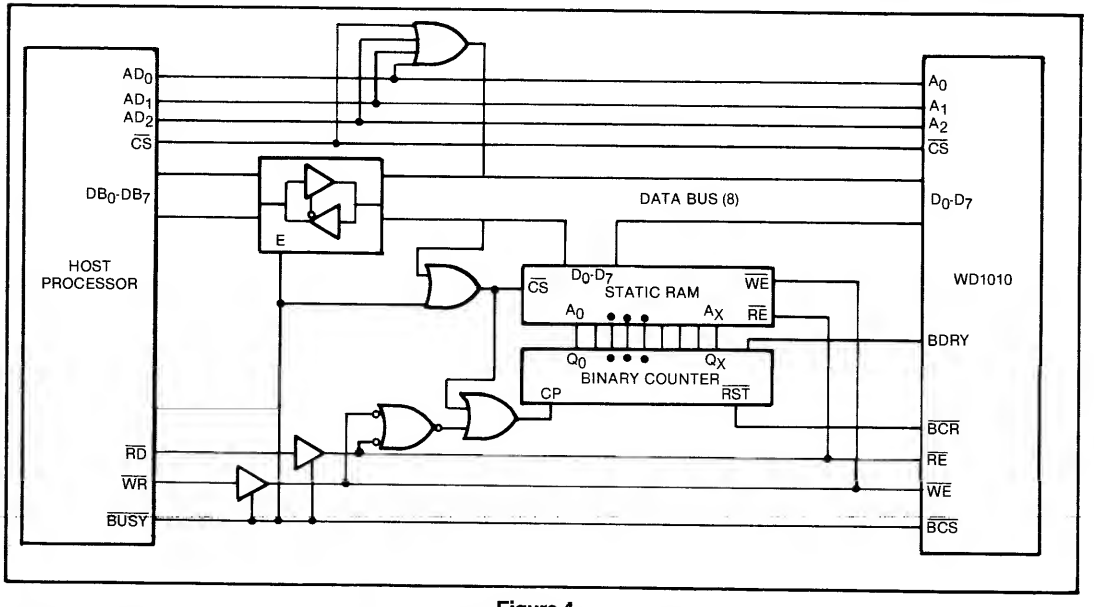


Figure 4.
Communications between a host and the WD1010 can be effected with the static RAM and binary counter circuitry shown here. These devices form a sector buffer that stores data sent from the host or the controller. This hardware handles both read and write operations on multiple sectors.

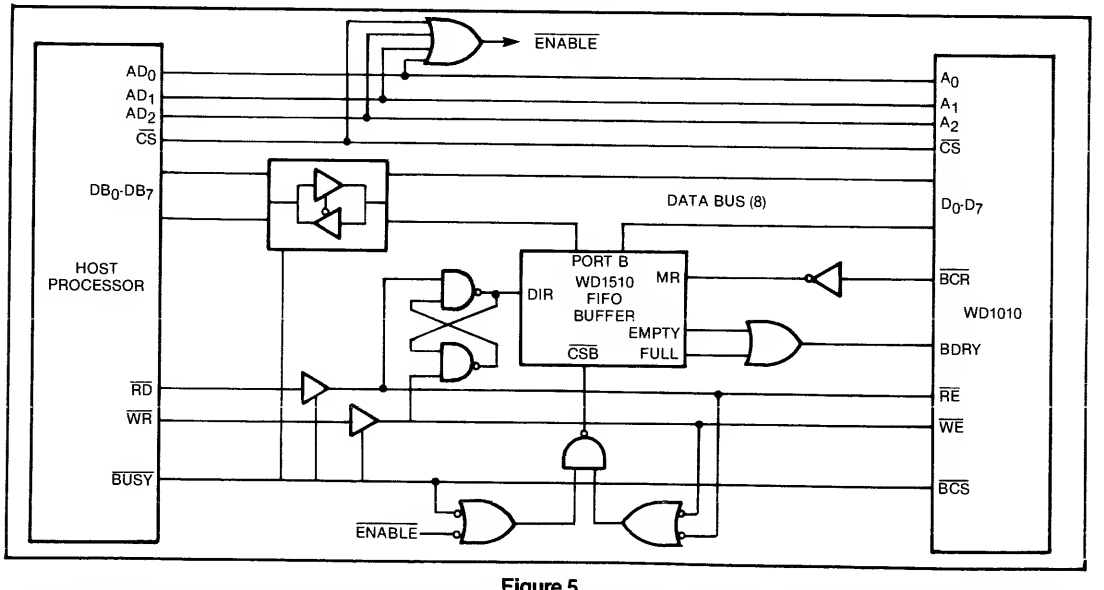


Figure 5.
A variation on the circuit of Figure 6 uses a WD1510 FIFO buffer to replace the counter-RAM circuitry. The scheme works well at high throughout rates since the buffer need not be filled to transfer data supplied by the WD1010 to the host.

bus and Read and Write lines from the WD1010. The Read ($\overline{RE}$) and Write ($\overline{WR}$) lines become outputs from the WD1010 and are strobed as each byte is placed on the bus.

The sector buffer in Figure 6 is implemented with a binary counter and a static RAM. With each $\overline{RE}$ or $\overline{WE}$ strobe, the counter is incremented so that the following byte can be read from or written to the next sequential location in the RAM. After all memory locations are written to, a carry signal from the counter goes to the Buffer Ready (BRDY) line of the WD1010. This signal informs the controller that the counter has rolled over and that the buffer is either full or empty, depending on the command.

During multiple-sector transfers, the RAM can be as large as the available sectors on each cylinder. The controller continues to load the RAM with data when a sector is being read. When no more memory is available. BRDY signals the WD1010. The command will then pause, wait for the host to dump the memory, and then begin filling the RAM again. This scheme permits both read and write operations on multiple sectors.

Signals for host and buffer control include the Buffer Counter Reset ($\overline{BCR}$) line, which is pulsed when $\overline{BCS}$ makes an active transition. $\overline{BCR}$ resets the binary counter before a read or write operation. Since address location 000 does not exist in the WD1010, a decoder can be used to make this address location enable the RAM and simulate a data register. For DMA applications, the Buffer Data Request (BRDQ) line is activated when data is available for host use.

Numerous other methods can be used with these same control signals. For example, a first-in, first-out buffer (Figure 7) can replace the counter-RAM. In this scheme, the host can dump data before the WD1010 fills the buffer. With sufficient throughput, the FIFO buffer need not have the storage capacity of an entire sector if the host can empty it quickly enough with a burst mode. In that case, the BRDY signal becomes the OR function of the Empty and Full signals from the FIFO buffer.

MACRO COMMANDS PROVIDE MULTIPLE OPTIONS

Each of the WD1010 Winchester controller-formatter's six macro commands contains several option flags. These flags allow the selection of stepping rates, multiple-sector transfers, and interrupt timing. The WD1010's task file contains additional options that are programmed before the command is actually issued. The operations of each command are as follows:

Restore causes the read/write head assembly to move to track 000. The stepping rate is determined by the state of Seek Complete (pin 32), which is activated by the drive to indicate its readiness. The stepping rate specified in the Restore command is not actually used but retained internally for an implied seek later on.

Activation of a Seek causes a seek operation for any desired cylinder. The selected cylinder is loaded into the cylinder register. Then the controller decides which way to seek and how many steps to use. The Seek Complete line is not checked, making possible overlapping seek operations on several drives.

The actual transfer of data from the WD1010 to sector buffer is performed under the Read Sector command. This command also causes a search for the specified cylinder, drive, head, and sector. Multiple sectors are specified and enabled through the sector count register. If the multiple-option flag is set, the number of sectors specified are transferred to the buffer.

Data in the sector buffer is written on the disk under the Write Sector command. Like the Read Sector command, it specifies and enables multiple drives through the sector count register.

Both the Read and Write Sector commands will retry up to eight times before automatically performing a restore operation. After a restoration, the controller seeks out the marginal sector and tries to determine whether an error condition was caused by a mispositioning of the head or a problem in the actuator.

The Format command is used to initialize a track with ID fields, gaps, and all information necessary for subsequent read and write operations. The sector buffer plays a unique role in this command, since it provides information on error mapping and inter-leaving rather than data from a sector. The order in which each sector is to be recorded is specified in the buffer, together with information indicating whether a sector contains a bad block or an error flag. Gap sizes, number of sectors, and other information are specified in the task file to allow further control over the format. By incrementing the cylinder number register, an entire surface can be formatted by accessing just two registers.

THE WD1010'S MACRO COMMANDS

	CODE							
	7	6	5	4	3	2	1	0
Restore	0	0	0	1	R_3	R_2	R_1	R_0
Seek	0	1	1	1	R_3	R_2	R_1	R_0
Read Sector	0	0	1	0	1	M	0	0
Write Sector	0	0	1	1	0	M	0	0
Scan ID	0	1	0	0	0	0	0	0
Write Format	0	1	0	1	0	0	0	0

M = Multiple Sector Flag

M = 0 — transfer 1 sector
M = 1 — transfer multiple sectors

I = Interrupt Enable

I = 0 — Interrupt at BDRQ time
I = 1 — Interrupt at end of command

A MULTIPLE-DRIVE SYSTEM

For multiple drive-head configurations, the WD1010's sector-drive-head (SDH) register is decoded at address 110 to produce individual, latched drive-selection signals whenever the host writes to this address location. Binary head selection does not require a separate decoder, since one is located at the drive.

When the WD1010 senses a change in drive number, it automatically reads a cylinder. This takes place before the execution of the current command. The chip records the new cylinder number it has read and stores it internally as a reference for future seek operations on the current drive.

After the execution of any command, the WD1010 informs the host processor of any errors encountered during execution. On-board status and error registers report error conditions and signal status from the drive. To eliminate tedious error detection procedures, the host processor need only check the error bit in the status register to determine whether any bits are set in the error register.

Bit 0 of the status register is set if any of 5 bits in the 8-bit error register are set — bit 0 establishes the logical OR of the status register. Other error indicators include a Bad Block Detect bit, which is activated when an ID field contains a bad block mark, and an ID Not Found bit, which is set when the desired cylinder, head, sector, or size parameter is not found after 16 revolutions of the disk. The latter is also set if the data address mark of the data field is incorrect when a read is executed.

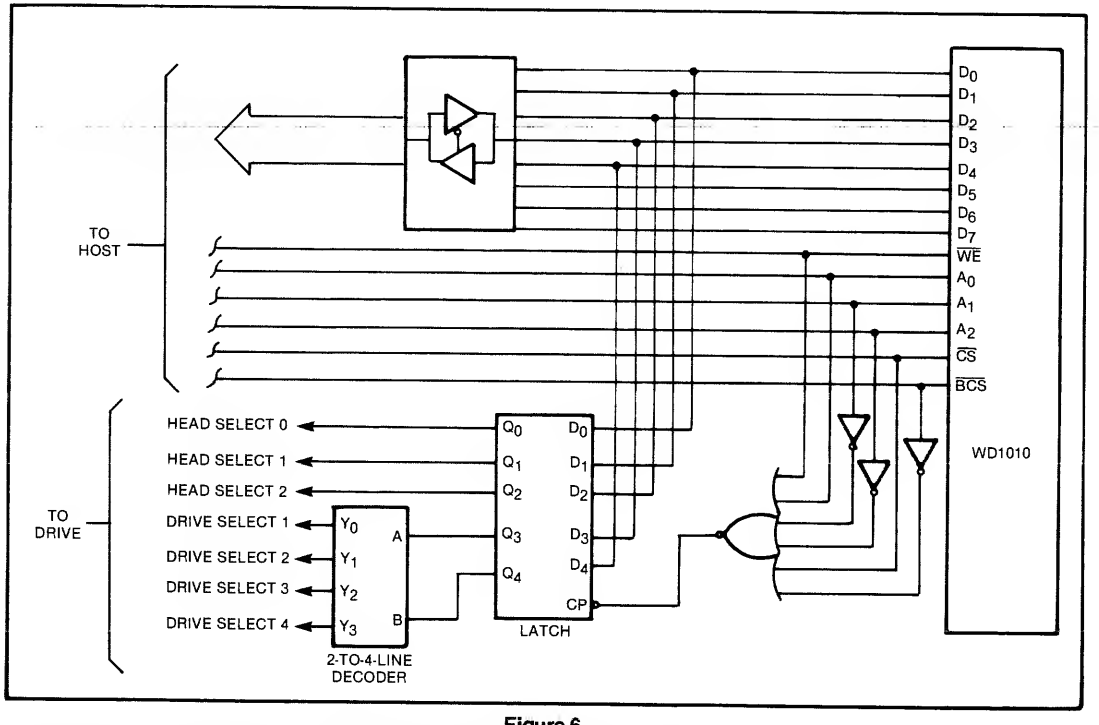


Figure 6.
Four Winchester drives can be controlled by the WD1010 using an external latch and a 2-to-4-line decoder. If the drive being accessed changes, the controller performs an automatic read operation. It records the cylinder number of the read for future seeks.

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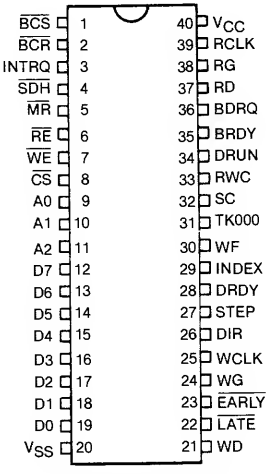
ADVANCED INFORMATION

WD2010 Winchester Disk Controller

FEATURES

- COMPATIBLE VIA 8-BIT DATA BUS WITH MOST MICROPROCESSORS
- UP TO 5 MBITS/S DATA RATE WITH AUTOMATIC ERROR CORRECTION
- MULTIPLE SECTOR READ/WRITE COMMANDS
- FORMATTING AND SECTOR INTERLEAVE CAPABILITY
- SEEK COMBINED WITH READ/WRITE COMMANDS
- SINGLE OR MULTIPLE SECTOR BUFFER USING FIFO OR RAM/COUNTER
- BUFFER ACCESS VIA PROGRAMMED I/O OR DMA
- 32 BIT ECC OR 16 BIT CRC SELECTABLE
- SELECTABLE 128, 256, 512, OR 1024 BYTE LENGTH SECTORS
- PROGRAMMABLE RETRY ALGORITHM
- SINGLE +5V SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD2010 Winchester Disk Controller is a single chip controller designed for use with the Shugart Associates SA1000 8" Winchester disk drive or the Seagate Technology ST506 5.25" Winchester disk drive. The WD2010 is designed to be software compatible with the WD1010. The WD2010 will read or write MFM data at a rate of up to 5 Mbits per second, with selected parts at a rate of up to 10 Mbits per second.

The WD2010 interfaces directly with TTL logic, is packaged in a 40-pin DIP, and requires only a single +5V supply. The WD2010 is designed to operate with an external sector buffer memory, or with an external DMA controller. Data bytes are transferred to or from the buffer every 1.6 usec. with a 5 Mbit per second drive. The buffer may consist of either a WD1510 128x9 FIFO memory, or a combination of a 256x8 static RAM and an 8-bit resettable counter. The WD2010 generates counter control signals to minimize external gating. Buffer to CPU transfers may be made via programmed I/O or DMA. The WD2010 also generates handshake signals to control DMA operation for multiple sector transfers.

A 32-bit ECC (Error Correction Code) polynomial or a 16-bit CRC polynomial may be selected. If a RAM/Counter sector buffer is used, the WD2010 can be programmed to automatically access the sector buffer and correct the data in error.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	BUFFER CHIP SELECT	$\overline{BCS}$	Active low output used to enable reading or writing of the external sector buffer.
2	BUFFER COUNTER RESET	$\overline{BCR}$	Active low output that is strobed by the WD1010 prior to read/write operations. This pin is strobed whenever $\overline{BCS}$ changes state.
3	INTERRUPT REQUEST	INTRQ	Active high output which is set to a logic high in the completion of any command.
4	SDH LATCH ENABLE	$\overline{SDH}$	Provides a latch enable signal when the SDH register is addressed.
5	MASTER RESET	$\overline{MR}$	A logic low in this input will initialize all internal logic.
6	READ ENABLE	$\overline{RE}$	Tristate bidirectional line, used as an input for reading the task register and an output when WD1010 is reading the buffer.
7	WRITE ENABLE	$\overline{WE}$	Tristate bidirectional line used as an input for writing into the task register and as an output when the WD1010 is writing to the buffer.
8	CHIP SELECT	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
9-11	ADDRESS 0 - ADDRESS 2	A0-A2	These three inputs select the register to receive/transmit data on D0-D7.
12-19	DATA 7 - DATA 0	D7-D0	Eight bit bidirectional bus used for transfer of commands, status, and data.
20	GROUND	V_{SS}	Ground.
21	WRITE DATA	WD	This output contains the MFM clock and data pulses to be written on the disk.
23, 22	LATE, EARLY	$\overline{LATE}$, $\overline{EARLY}$	Precompensation outputs used to delay the WD pulses externally.
24	WRITE GATE	WG	This output is set to a logic high before writing is to be performed on the disk.
25	WRITE CLOCK	WC	4.34 or 5.0 Mhz clock input used to derive all internal write timing.
26	DIRECTION	DIR	This output determines the direction of the stepping motor.
27	STEP PULSE	STEP	This output generates a pulse for stepping the drive motor.
28	DRIVE READY	DRDY	This input must be at a logic high in order for commands to execute.
29	INDEX PULSE	INDEX	A logic high on this input informs the WD1010 when the index hole has been encountered.
30	WRITE FAULT	WF	An error input to the WD1010 which indicates a fault condition at the drive.
31	TRACK 000	TK000	An input to the WD1010 which indicates positioning over track 000.
32	SEEK COMPLETE	SC	This input informs the WD1010 when head settling time has expired.
33	REDUCED WRITE CURRENT	RWC	This output can be programmed to reduce write current on a selected starting cylinder.

PIN DESCRIPTION (CONT.)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
34	DATA RUN	DRUN	This input informs the WD1010 when a field of one's or zeroes have been detected.
35	BUFFER READY	BRDY	This input is used to inform the controller that the sector buffer is full or empty.
36	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the sector buffer.
37	READ DATA	RD	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
38	READ GATE	RG	This output is set to a logic high when data is being inspected from the disk.
39	READ CLOCK	RC	A nominal square wave clock input derived from the external data recovery circuits.
40	+5 VOLT	V_{CC}	+5V ±5% Power supply input.

See page 481 for ordering information.

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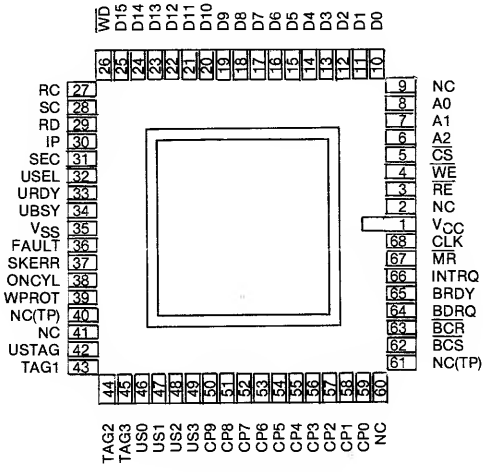
WESTERN DIGITAL
CORPORATION

WD1050 SMD Controller/Formatter

FEATURES

- 16 BIT HOST INTERFACE
- 9.677 MBITS/SEC DATA RATE
- SINGLE/MULTIPLE SECTOR TRANSFERS
- FIXED SECTOR FORMAT
- TTL COMPATIBLE INPUT/OUTPUTS
- SINGLE 5V SUPPLY
- 68 PIN JEDEC TYPE C CHIP CARRIER PACKAGE
- COMPATIBLE WITH SMD, MMD, FHT, LMD, AND CMD FAMILIES
- SINGLE +5V SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1050 SMD controller/formatter is a MOS/LSI device designed to interface an SMD compatible rigid disk drive to a host processor. The device is compatible with all rigid disk drives adhering to Control Data Corporation's flat cable interface for SMD, MMD, FHT, FMD, LMD and CMD families (CDC specification 64712400 Rev H). It is TTL compatible on all inputs and outputs, with interface capability for 8 or 16 bit data busses.

The WD1050 contains a powerful set of macro-commands for read/write and control functions. An internal 16 bit task file is used to process a selected command based upon parameter information in the file.

The WD1050 operates from a single +5V supply and is available in a 68 pin JEDEC Type C chip-carrier package.

PIN NUMBER	NAME	SYMBOL	DESCRIPTION
1	V_{CC}	V_{CC}	+5V ±5% power supply input
2	NO CONNECTION	NC	
3	$\overline{\text{READ ENABLE}}$	$\overline{RE}$	Tri-state bidirectional line, used as an input when reading the task file and an output when the WD1050 is reading from the buffer.
4	$\overline{\text{WRITE ENABLE}}$	$\overline{WE}$	Tri-state bidirectional line used as an input when writing to the task file and an output when the WD1050 is writing to the buffer.
5	$\overline{\text{CHIP SELECT}}$	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals as inputs.
6-8	ADDRESS 0-2	A_0-A_2	These three inputs select a task file register to receive/transmit data.
9	NO CONNECTION	NC	
10-25	DATA BUS 0-15	D_0-D_{15}	Sixteen bit bidirectional bus used for transfer of commands, status, and data.
26	$\overline{\text{WRITE DATA}}$	$\overline{WD}$	Open drain, NRZ data output which is synchronized to the Servo Clock input.
27	READ CLOCK	RCLK	Input clock from the drive which is synchronized with the Read Data Input.
28	SERVO CLOCK	SCLK	A nominal 9.677 MHz clock input from the drive. This clock must be valid when Unit Ready (Pin 31) is active and Fault (Pin 34) is inactive.
29	READ DATA	RD	NRZ data input from the drive which must be synchronized to the Read Clock (Pin 25) input.
30	INDEX PULSE	IP	Active high input used to monitor the Index signal from the drive.
31	SECTOR	SEC	Active high input used to monitor sector pulses from the drive.
32	UNIT SELECTED	USEL	Active high input used to verify the selected drive.
33	UNIT READY	URDY	Active high input used to inform the WD1050 of a ready condition on a selected drive. If this line is made inactive during any command (except RTZ or FAULT CLEAR), command execution is terminated.
34	UNIT BUSY	UBSY	Active high input used to monitor drive status during a unit selection. If the unit had previously been selected and/ or reserved prior to issuing a USTAG, the UBSY must be made active within one microsecond of the USTAG selection. This signal is used for dual-channel access applications and should be tied to ground when not used.
35	GROUND	V_{SS}	Ground.
36	FAULT	FAULT	Active high input used to detect a fault condition at the drive. Command execution is terminated if Fault is made active during any command. Only the FAULT CLEAR command may be issued while this line is asserted.

PIN NUMBER	NAME	SYMBOL	DESCRIPTION
37	SEEK ERROR	SKERR	Active high input used to detect a seek error at the drive.
38	ON CYLINDER	ONCYL	Active high input used to inform the WD1050 when the heads are settled and positioned over a cylinder.
39	WRITE PROTECT	WPROT	Active high input used to monitor the Write Protect signal from the drive.
40	NO CONNECTION	NC(TP)	Test point.
41	NO CONNECTION	NC	
42	UNIT SELECT TAG	USTAG	Active high output used for selection of a unit on US0-US3 lines.
43-45	TAG1-TAG3	TAG1-TAG3	Active high outputs used to strobe specific data out on the Control Port Lines. Tag definitions are: TAG1 — Cylinder address TAG2 — Head/Volume select TAG3 — Control Tag
46-49	UNIT SELECT 0-3	US0-US3	These four outputs reflect the contents of the unit address field of the task file and are used to select one of 16 drives.
50-59	CONTROL PORT BITS 9-0	CP9-CP0	Ten bit output bus used to issue tag parameters to the selected drive.
60	NO CONNECTION	NC	
61	NO CONNECTION	NC(TP)	Test point.
62	$\overline{\text{BUFFER CHIP SELECT}}$	$\overline{\text{BCS}}$	Active low output used to enable reading or writing to the external buffer by the WD1050.
63	$\overline{\text{BUFFER COUNTER RESET}}$	$\overline{\text{BCR}}$	Active low output that is strobed prior to read/write commands. Used to clear an external buffer counter.
64	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the external buffer.
65	BUFFER READY	BRDY	This input informs the WD1050 that the buffer is either full or empty.
66	INTERRUPT REQUEST	INTRQ	Active high output which is set at the completion of any command, providing the 'I' bit is also set in the command word. INTRQ is reset subsequent to a Status register read.
67	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	Active low input used to initialize the WD1050, usually after a power-up condition.
68	CLOCK	CLK	2 MHz Master Clock is input.

FUNCTION DESCRIPTION

The WD1050 SMD Winchester Controller performs the necessary link between an 8 or 16 bit processor and an SMD compatible drive. The internal architecture of the WD1050 is shown in Figure 1. The major functional blocks are:

Control Unit

This section decodes commands, implements command execution sequencing, monitors the comparator and CRC logic, monitors status and issues control to the Host and Drive Interfaces. It also writes appropriate information to the Status register during command execution.

Data I/O Buffers

A 16-bit bi-directional three-state bus (D15-D0) for data transfers between the host CPU or data buffer and the HDC. (The higher order 8-bits of this bus [D15-D8] may be used for 8-bit data bus transfers between the host CPU and the HDC).

Host/Buffer Control

This section allows HDC register selection and communication by the CPU, issues interrupt requests, and provides Direct Buffer Access (DBA) transfers between the disk drive and the data buffer.

Status Register

A 16-bit register reflecting operational status of the HDC and disk drive. This is a read-only register.

Command Register

A 16-bit field containing command information that dictates operational control sequencing of the Host and Drive Interfaces by the HDC. This is a write-only register.

Data Register

A 16-bit field used to assemble/disassemble words/bytes during data transfers. This register is internally interfaced to the HDC's Data I/O Buffers ('D' bus) and the HDC's Read Data Holding (RDH) register or Write Data Holding (WDH) register (as appropriate) during host/drive data transfers. The contents of this register are compared to the appropriate Task File field as required by command execution.

CRC Logic

This logic is used to generate or check the 16-bit Cyclic Redundancy Check (CRC). The polynominal is:

$$G(x) = X^{16} + X^{12} + X^5 + 1$$

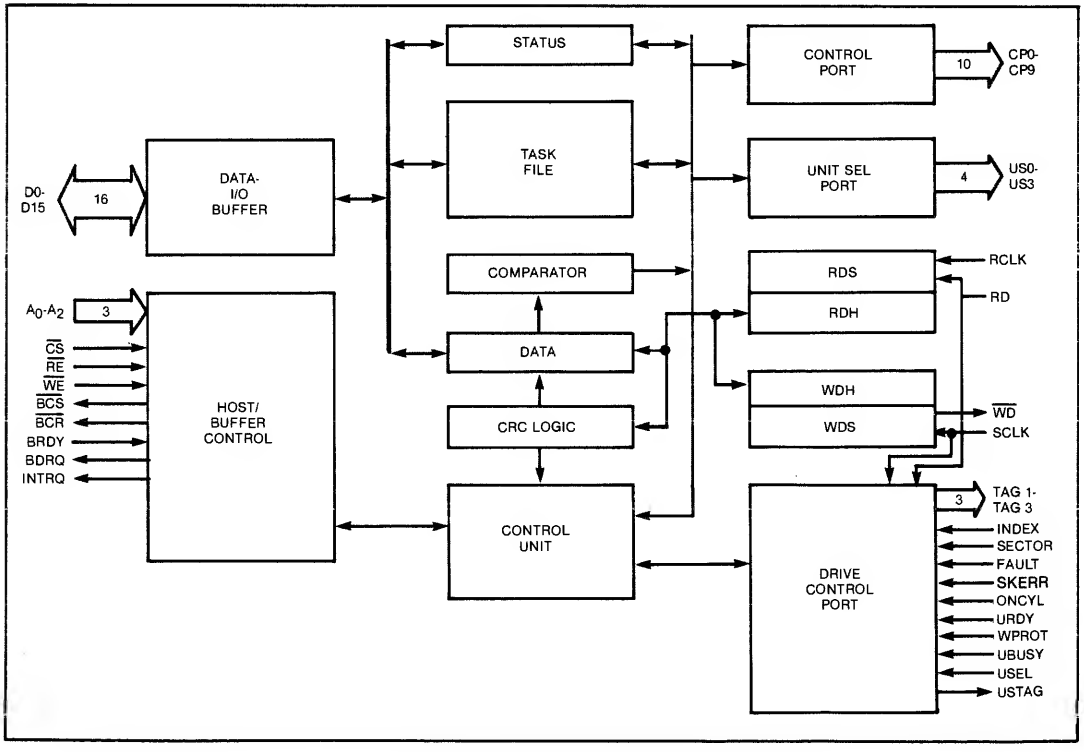


Figure 1. BLOCK DIAGRAM

The CRC includes all information beginning with the Sync character and ending with the CRC word. The CRC is preset to ones prior to a data transmission.

The CRC is implemented in parallel eight bits at a time as data is transferred between the HDC's Data register and the HDC's Read or Write Data Holding registers. The CRC word is transferred to the HDC's Data register and appended to the ID Field and Data Field (if enabled) during Format Sector or Write Data Commands.

Comparator

A 16-bit comparator used to compare the appropriate HDC's Task File field with the respective byte(s) read from the disk.

Read Data Shift Register (RDS)

This 8-bit register shifts data read from Read Data (RD) input via the drives Read Clock (HDC's RCLK input).

Read Data Holding Register (RDH)

This 8-bit holding register assembles bytes from the Read Data Shift register and transfers them to the Data register.

Write Data Holding Register (WDH)

This 8-bit holding register receives bytes from the Data register and provides an eight bit parallel input to the HDC's Write Data Shift register (WDS).

Write Data Shift Register (WDS)

This 8-bit shift register converts the eight bit parallel input from the Write Data Holding register (WDH) into a serial bit stream issued to the HDC's Write Data ($\overline{WD}$) output via the drive's Servo Clock (HDC's SCLK input).

Drive Control

This section monitors drive status, synchronizes the byte boundries generated by the Serve Clock to the sync character read from the disk or the drive's Index or Sector pulse as appropriate, and issues control tags to the drive.

Control Port (CP0-9)

This 10 bit output port is used to provide the drive with volume/head #, cylinder address, and control information in conjunction with outputs Tag 1 (cylinder address), Tag 2 (volume/head #), and Tag 3 (control). The contents of the appropriate HDC register or signals generated from the Control Unit are gated to the Control Port during command execution.

Unit Select Port (US0-3)

This 4-bit output port reflects the contents of the Unit Address register, respectively. The Unit Select Tag output selects the desired disk drive unit.

HOST INTERFACE

The primary interface between the Host processor and the WD1050 is through a 16-bit bi-directional bus. This bus is used to transfer status, parameter, and command information between the WD1050 and the host, as well as data between the WD1050 and sector buffer. The external sector buffer is constructed with either FIFO memory or a RAM and binary counter. Since the WD1050 will make this bus active when accessing the sector buffer, a transceiver must be used to isolate this bus from the host. Figure 2 shows a typical Host Interface using a RAM and Binary counter. The sector buffer may be one or more sectors in length, depending upon system requirements.

Whenever the WD1050 is not using the sector buffer, the Buffer Chip Select ($\overline{BCS}$) is high (disabled). This allows the Host to access the WD1050's Task File, read status, and issue commands. It also allows the host to access data within the sector buffer. A separate RAM select line from the host is used to access the data in memory. With each $\overline{RE}$ or $\overline{WE}$ strobe from the host, the address counter is incremented on the trailing edge of $\overline{RE}$ or $\overline{WE}$, pointing to the next sequential memory location. Whenever the WD1050 changes the state of $\overline{BCS}$, the Buffer Counter Reset ($\overline{BCR}$) Line is strobed, causing the address counter to be reset to zero. The $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1050 to allow access to the buffer only when $\overline{BCS}$ is low. Although 8-bit programming is allowed via the use of Address Line 0, the data path to and from the WD1050 must be 16 bits wide.

TASK FILE

The WD1050 contains five 16-bit registers called the Task File. These registers are used to set up parameter information prior to issuing a command. These registers are:

A2	A1	A0	15 REGISTER 0
0	0	0	HEAD/SECTOR ADDRESS
0	1	0	SECTOR COUNT/LENGTH & UNIT ADDRESS
1	0	0	CYLINDER REGISTER
1	1	0	COMMAND REGISTER (WRITE ONLY)
1	1	0	STATUS REGISTER (READ ONLY)

Each register in the Task File is accessed by selecting the proper address while $\overline{CS}$ (pin 4) is low, then strobing the $\overline{WE}$ or $\overline{RE}$ lines. All registers in the Task File are Read/Write except for the Command/Status register. The Command register can only be written to, while the Status register is a read-only register. But the command and status registers have the same address.

An 8-bit mode can also be used for accessing the Task File. Data is read/written on the most significant

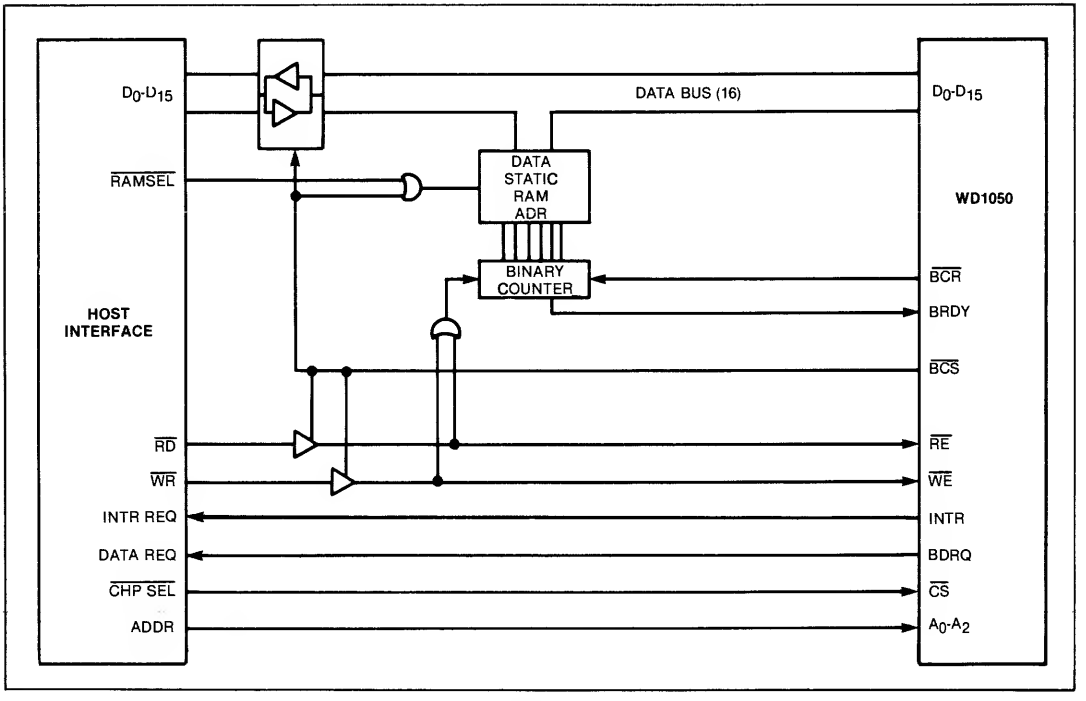
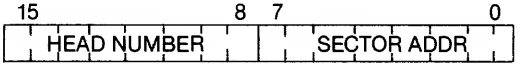


Figure 2.

8-bits of the Data bus (D15-D8). The upper byte is accessed when A_0 (pin 7) is high, and the lower byte is accessed when A_0 is low. The upper byte ($A_0 = 1$) must be accessed first, followed by the lower byte. This insures that data is transferred to the internal 16 bit bus properly, and that a command will execute when the full 16 bit word is written.

Head/Sector Address

This register holds the Head number and sector address fields:



The Sector Address byte (bits 7-0) holds the logical sector number used for comparison when searching for the specified ID field. The Head number byte (bits 15-8) hold the logical head number, and volume flag (where applicable). This 8 bit field is sent to the drive via the Control Port (CP7-0) when Tag 2 is issued. Note that all 8 bits of each byte are written into the ID field during formats and are compared during other commands.

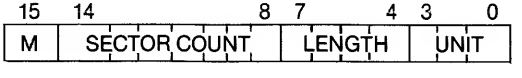
Cylinder Register

This Register holds the 16 bit cylinder number:

The least significant 10 bits of this register (bits 9-0) are transferred to the Control Port (CP9-0) when Tag 1 is issued. All sixteen bits of this register are written to the ID field during formats and are compared during other commands.

Sector Count/Length & Unit Address

This register holds the sector count, sector length and unit address fields:



The four bit unit address field (bits 3-0) contains the physical unit address and is reflected at the drive via the Unit Select Port (US3-0). This port is used in conjunction with the Unit Select Tag (USTAG) output to select the desired drive.

The four bit sector length field is used to determine the number of bytes to be read/written from the disk. The allowable sector lengths are:

BITS 7	6	5	4	# OF BYTES IN DATA FIELD
1	0	0	0	128
0	1	0	0	256
0	0	1	0	512
0	0	0	1	1024

If the CE bit (CRC Enable) in the command word is zero, an additional 8 bytes are added to the above sector lengths (and the CRC bytes are not appended to the data field). These bytes can be used to append ECC codes to each sector.

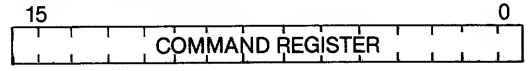
The Sector Count Field, seven bits of which (bits 14-8) are used to control single/multiple record operation for commands where the LS (Logical Sector) Flag is set, is decremented by one for each sector encountered after the desired sector has been located on the disk. The Op Code command is repeated until the contents of this field (bits 14-8) are equal to zero. For single sector operation, this field (bits 14-8) must equal "0000000." (This field [bits 14-8] is ignored for the Fault Clear command).

For the Format Sector, Verify Sector, and commands where the LS flag is not set, the Sector Count Field (bits 14-8) must contain the desired physical sector location (i.e., the Sector Count number of sector pulses from the Index pulse = physical sector location). This register is counted down to zero to determine the physical sector location for these commands. For physical sectored commands, bit 15 is used as a one bit field controlling single/multiple record operation. For bit 15 equal to '0', a single sector command is executed. For bit 15 equal to '1', these commands are repeated until the Index pulse is re-encountered, allowing multiple sector operations.

For logical sectoring, bit 15 of this register should equal '0.'

Command Register

This "write-only" register is used to load in the desired command:



The command register may be loaded whenever the Command-In-Process (CIP) status bit is reset.

Status Register

This "read-only" register is used to monitor status and error conditions as the result of command execution. Its format is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCS	CIP	UBSY	USEL	WPRT	URDY	OCYL	SKER	BCS	FLT	BDRQ	—	DFCE	DFNF	IDCE	IDNF

BIT	NAME	DESCRIPTION
0	ID Field Not Found (ID/NF)	Set if the sync character preceding the ID Field or ID Field contents read from the disk do not match the respective Task File contents.
1	ID CRC Error (IDCE)	Set if the CRC calculation on the ID Field read from the disk is in error.
2	Data Field Not Found (DFNF)	Set if the Data Field sync pattern following the ID Field does not match the sync character.
3	Data Field CRC Error (DFCE)	Set if the CRC Calculation on the Data Field read from the disk is in error.
4	Not Used	This bit is not used; it is forced to a zero.
5	Buffer Data Request (BDRQ)	Reflects the Buffer Data Request output.
6	Fault (FLT)	Reflects the status of the Fault (Flt) input.
7	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select ($\overline{BCS}$) output.
8	Seek Error (SKER)	Reflects the status of the Seek Error (Sk Er) input.
9	On Cylinder (OCYL)	Reflects the status of the On Cylinder (On Cyl) input.
10	Unit Ready (URDY)	Reflects the status of the Unit Ready (U Rdy) input.
11	Write Protect (WPRT)	Reflects the status of the Write Protect (WPRT).
12	Unit Selected (USEL)	Reflects the status of the Unit Selected (U Sel) input.
13	Unit Busy (U Bsy)	Reflects the status of the Unit Busy (U Bsy) input.
14	CIP	Set when a command is in progress.
15	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select ($\overline{BCS}$) output. This bit also appears in STATUS Bit 7.

INSTRUCTION SET

The WD1050 will execute eight commands. Prior to issuing a command, the Host must first setup the Task File with parameter information. A command can only be accepted if the CIP bit in the status register is reset.

COMMAND	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
	COMMAND REGISTER BITS															
Fault Clear	1	0	0	0	0	0	0	I	0	0	0	0	U	S	E	D
Return to Zero	1	0	0	1	0	0	0	I	0	0	0	M	U	S	E	D
Seek Cylinder	1	0	1	0	V	L	O	I	Z	C	H	M	U	S	E	D
Read ID Field	1	0	1	1	R	L	O	I	Z	C	H	M	U	S	E	D
Read Sector	1	1	0	0	R	L	O	I	Z	C	H	M	U	S	E	D
Write Sector	1	1	0	1	R	L	O	I	Z	C	H	0	U	S	E	D
Format	1	1	1	0	R	P	O	I	Z	C	H	0	U	S	E	D
Verify	1	1	1	1	R	P	O	I	Z	C	H	M	U	S	E	D

FLAG SUMMARY

V	= Verify	I	= Interrupt Enable
R	= CRC Enable	Z	= Volume/Head Change
L	= Logical Sectoring	C	= Cylinder Addr
P	= Programmable Sectors	H	= Head Selection
O	= On Cylinder	M	= Marginal Data Recovery
E	= Priority Release/Early	U	= Unit Sel/Servo Minus
D	= Unit Deselect/Late	S	= Priority Sel/Servo Plus

COMMAND FLAG DESCRIPTION

FLAG	NAME	DESCRIPTION
V	Verify	Compare the Head number and Cylinder Address word of the ID field with the appropriate Task File field when On Cylinder becomes active. The Sector Address byte in the ID Field is not compared, although the CRC is checked. This flag is valid only for the Seek Cylinder command.
R	Data Field CRC Enable	Data Field CRC is enabled. If the flag is **not** set, the condition of the DFCRC Status bit will not affect command execution; the data field is extended by four words (8 bytes), and the CRC bytes are not appended.
L	Logical Sectoring	Locate sector by matching the ID Field bytes read from the disk to the appropriate field in the HDC Task File. The Sector Count register in the Task File is used to indicate the additional number of sectors to be transferred for multiple sector commands. If L is **not** set, physical sectoring is implemented. The Task File Sector Count register is decremented to locate the desired physical sector from the Index pulse. ID Field compares are made, but do not affect command execution.
P	Programmable Sectors	The Head Number/Sector Address register is read from the buffer as each sector is encountered per command execution. (This allows an entire track to be formatted/verified with interleave sectors in one revolution of the disk). This flag is valid only for the Format Sector or Verify Sector commands.
O	On Cylinder	For the Seek Cylinder command, command completion requires activation of On Cylinder or Seek Error inputs. For other commands, On Cylinder is required before a read or write can occur.
I	Interrupt Enable	Enable the interrupt output (INTRQ) for activation upon completion or termination of command execution.

COMMAND FLAG DESCRIPTION

FLAG	NAME	DESCRIPTION
Z	Volume/Head	Issue Tag 2 as required for volume/head change.
C	Cylinder	Issue Tag 1 as required for cylinder address selection. (Tag 1 will follow Tag 2 if the Z and C flags are both set).
H	Head	Issue Tag 2 as required for head selection. (Tag 2 will follow Tag 1 if the C and H flags are both set).
M	Marginal Data	Attempt a marginal data recovery. (Marginal data recovery may be attempted only where a command requires reading from the drive). This bit controls the function of bits 3-0 (U, S, E, D). (See Note 1).
U	Unit Select/Servo Offset Minus	For M = 0 (or not applicable), set Unit Select Tag as required for unit selection. Unit Selected must become active for command execution to continue. For M = 1, issue servo offset minus control for marginal data recovery attempt.
S	Priority Select/ Servo Offset Plus	For M = 0, issue priority select control as required to reserve the unit. (See Note 2). For M = 1, issue servo offset plus control for marginal data recovery attempt.
E	Priority Release/ Data Strobe Early	For M = 0, issue priority release control as required to release reserve of the unit. (See Note 2). For M = 1, issue data strobe early control for marginal data recovery attempt.
D	Unit Deselect/Data Strobe Late	For M = 0, reset Unit Select Tag at completion of this command. For M = 1, issue data strobe late control for marginal data recovery attempt.

Note 1: Certain marginnal data recovery features are not applicable depending on the particular drive type under control. (Refer to CDC Interface Specification 64712400).

Note 2: Priority select and release features are applicable only for dual channel drive applications.

COMMAND EXECUTION

Command word architecture has been designed to provide comprehensive control of the drive unit via programmable micro-level commands. For example, unit selections, cylinder seek, head selection, Op Code execution (of multiple records if desired), and unit deselection can be performed with a single command.

Command execution follows the following sequence (for 'M' flag = 0):

1. If the U flag is set, the Unit Select (US) Tag is activated. (The drive should select the unit specified by the Unit Select bus [US0-3] when the US Tag is activated.)

   If the S flag is also set, CP9 will be active when the US Tag is activated (exclusively reserving the unit to that channel until released).

2. The following conditions must be met and maintained for command execution to continue:
   Unit Ready input active
   Unit Selected input active
   Unit Busy input not active

   If these conditions are not met, command execution is terminated with the appropriate bit set in the Status register.

   For all commands except the Fault Clear command, the Fault input must also be inactive and remain inactive for command execution to continue.

3. For the Write Data and Format Commands, the Write Protect Status bit is checked; if true command execution is terminated.

4. For the Write Data command, and the Format and Verify command with the P (programmable sector) flag set, the HDC activates BDRQ requesting the host to provide the required data to the buffer.

5. If the Z flag is set (indicating a volume change), the Head number field of the Task File is issued to the Control Port (Head field bits 15-8 to CP lines 7-0 respectively), and Tag 2 is pulsed. (Applies only for drives with volume select.)

6. If the C flag is set (indicating a cylinder address seek), the Cylinder Address field of the Task File is issued to the Control Port (bits 9-0 respectively), and Tag 1 is pulsed.

NOTE:
For the Seek Cylinder command, and for other commands where the On Cylinder flag is set, the On Cylinder input must be active before Tag 1 will be issued. (If the Seek Error input is active or becomes active before On Cylinder is active, execution is terminated with the Seek Error status recorded in the Status register.

7. If the H flag is set (indicating a head selection), the Head number field of the Task File is issued to the Control Port (Head field bits 15-8 to CP lines 7-0 respectively), and Tag 2 is pulsed.
8. For commands other than Seek Cylinder, O flag operation is as follows:

   If O is set, execution is suspended pending an active On Cylinder input.

   If O is not set, the command is executed regardless of the condition of On Cylinder.

   NOTE:
   Data transfer to/from the drive with On Cylinder inactive is allowed only under certain circumstances on specific drives. For example, on a drive with both fixed and moveable heads, it is possible to execute a Seek Cylinder command with the C flag not set to the moveable heads (On Cylinder will drop). The fixed heads may then be given a Read Data command with the O flag not set. The fixed head can then be read regardless of the condition of On Cylinder. (This is an overlap seek within a given unit between the fixed and moveable media). For valid read/write operation without an active On Cylinder, refer to the appropriate drive operating specification.

   For commands with C set and Seek Error received instead of On Cylinder, command execution is terminated.
9. For the Write Data command, and the Format and Verify commands with the P flag set, the BRDY input is inspected. Command execution is suspended pending reception of a low to high transition on the BRDY input.

   NOTE:
   For commands where M is set, marginal data recovery control as described in the chart below is issued to the control port prior to the activation of Tag 3. Note that unit selection, channel reserve control, and unit deselection must be accomplished with a non-marginal data recovery command since the U, S, E, and D flags assume marginal data recovery control significance.

MARGINAL DATA RECOVERY OPERATION

COMMAND FLAG IF MD IS SET	FEATURE	CONTROL PORT BIT ACTIVATED
U	Servo Offset Plus	2
S	Servo Offset Minus	3
E	Data Strobe Early	7
D	Data Strobe Late	8

Location of the appropriate sector within the cylinder is common to all commands except Fault Clear and RTZ. One of two methods is used: logical sector search (for commands where the L flag is set) and physical sector locating (for the Format and Verify commands and commands where the L bit is not set).

Logical sector search consists of reading the first encountered ID Field, comparing these bytes to the appropriate fields in the HDC's Task File, (including the sync byte) and checking the ID Field CRC bytes. When a valid compare with correct CRC are found, execution continues. If a valid compare with correct CRC are not found before four Index pulses are detected, the appropriate Status bits are set (IDNF and/or IDCE) and command execution is complete. For multiple sector commands, the Sector Address field of the Task File is incremented between sectors and the Sector Count field is used to indicate the number of additional sectors for which the command is to be executed. A single sector command is executed for Sector Count = '00 . . . 00'.

Physical sector locating is accomplished by decrementing the Sector Count field of the Task File by one for each Sector pulse encountered after the Index pulse is located until the Sector Count field = '0000000'. For Sector Count = '0000000', the command will be executed to the sector immediately following the Index pulse). The ID Field compares and the IDCE check are still made and the appropriate bit set in the Status register (if applicable), but command execution is not affected by an error condition. A single sector command is executed if bit 15 of the Sector Count/Sector Length/Unit Address register of the Task File is zero. If bit 15 is one, command execution is repeated until the Index pulse is re-encountered. Note that Status register error bits are not cleared between sectors (one's catching).

Tag 3 (Control Select) is activated for all commands except Seek Cylinder with the V flag not set.

When the appropriate Sector pulse is encountered, CPI (Read Gate) is activated and the HDC synchronizes to the first low to high transition on the Read Data (RD) input. This initiates the following three compares: the sync byte FE preceded by eight zeros, the upper and lower Cylinder Address, and the Head number and Sector Address. (The Sector Address compare is suppressed on the RTZ and Seek Cylinder commands). The ID FIELD CRC is then checked. CPI is deactivated and command execution follows.

FAULT CLEAR

CP4 (Fault Clear) is pulsed and this completes execution. This command is intended to clear the Fault output of the drive. The condition causing the fault within the drive should no longer exist when this command is issued.

RTZ (RETURN TO ZERO)

CP6 (RTZ) is pulsed and the Cylinder Address, Head

number, and Sector Address fields of the Task File are all set to zero. This completes execution.

SEEK CYLINDER

Execution of this command is controlled completely by the command flags. If O is set, execution is suspended until On Cylinder (or Seek Error) is received. If the V flag is not set, receipt of On Cylinder completes execution. If C and V are both set, and On Cylinder is received, CPI (Read Data) is issued and the ID Field is inspected. The Sector Address compare is not made for this command.

NOTE:
If L is set (logical sectoring), execution is complete when ID Field is successfully found or when the 4th Index pulse is encountered. There is no multiple sector operation when L is set for this command. If L is not set (physical sectoring), the IDNF and IDCE Status bit are one's catching. (The entire track may be verified with multiple sector operation).

The V flag is ignored if the O flag is not set.

If the C flag is not set, this command may be used for Unit Select only functions.

READ ID FIELD

The Read ID Field command is provided to allow transfer of the ID Field formatted on the disk to the data buffer (ie., $\overline{BCS}$ • D15-D0 • $\overline{WE}$ pulses). The Sector Address field is not compared in this command.

If the L flag is set, the first encountered ID Field is transferred to the buffer. The following bytes are transferred: 00FE, Upper and Lower Cylinder Address, Head number, Sector Address, and the two CRC bytes. Thus four $\overline{WE}$ pulses are issued.

If the L flag is not set, the physical sector is located and the corresponding ID Field is transferred to the buffer.

There are no retries with this command if ID Field compare errors result.

CP1 is then reactivated, and the first low to high transition on the RD input causes a compare for the Data Field sync character. If the compare does not match, the Data Field Not Found (DFNF) Status bit is set. The Data Field CRC (DFCE) Status bit is set if an error is detected. CP1 is then deactivated.

Note that the Data Field is not transferred with this command.

For multiple sector operation, the Sector Address Field of the Task File is automatically incremented. The BRDY input is inspected following each sector's transfer. If a low to high transition has not occurred (ie., buffer not full) execution is then repeated. If a low to high transition has occurred, (ie., buffer is full) $\overline{BCS}$ is deactivated, $\overline{BCR}$ is pulsed, and BDRQ is activated. Execution is suspended pending a low to high transition of BRDY (ie., buffer empty). $\overline{BCR}$ is then pulsed, and execution is repeated. If a Data Field CRC is detected, the command will not terminate.

READ DATA

After the appropriate sector has been located, Data Field operation is as described under the Read ID Field Command, except that the Data Field is transferred to the buffer. Note that only the Data Field data bytes are transferred with this command.

This completes execution for single sector commands and for multiple sector commands where the L and R flags are set. If a Data Field sync error (DFNF) or a Data Field CRC (DFCE) error has occurred, the command will also be terminated.

For multiple sector command where the C flag and/or L flag is not set, and for multiple sector commands where no Data Field error has occurred, execution is repeated.

Note that if the R flag and/or the L flag is not set, the DFNF and DFCE Status bits are one's catching.

WRITE DATA

After the appropriate sector has been located, CP0 (Write Gate) is activated. Thirteen bytes of zeros (two Write Splice bytes and eleven PL0 Sync bytes) are written followed by the sync character. The Data Field is then written to the disk from the data buffer (ie., $\overline{BCS}$ • D15-D0 • $\overline{RE}$ pulses). The CRC bytes and two bytes of zeros (End of Record) are appended to the Data Field and written to the disk.

For multiple sector operation, the BRDY input is inspected following each sector's transfer. If a low to high transition has not occurred (ie., buffer not empty), execution is then repeated. If a low to high transition has occurred (ie., buffer empty), $\overline{BCS}$ is deactivated, $\overline{BCR}$ is pulsed, and BDRQ is activated. Execution is suspended pending a low to high transition on BRDY (ie., buffer full). $\overline{BCR}$ is then pulsed, and execution is repeated.

FORMAT SECTOR

Physical sectoring only applies to the Format Sector command. Upon reception of the appropriate Sector pulse, CP0 (Write Gate) is activated. Twenty seven bytes of zeros (16 Head Scatter bytes and eleven PL0 Sync bytes), and the sync character are written to the disk. The four ID Field bytes are written to the disk from the HDC's Task File, and the resultant CRC is appended. Thriteen bytes of zeros are written (two Write Splice bytes and eleven PL0 sync bytes) followed by the sync character. The Data Field (Format Character E5 repeated) is then written. If the R bit is set, then the two CRC bytes are appended; if R is not set eight additional E5's are added to the data field. Zeros are written until the next Sector or Index pulse is encountered.

For single sector operations CP0 is then deactivated.

For multiple sector operation, CP0 remains active, and execution is repeated until the Index pulse is again encountered.

If the P flag is set, the HDC will fetch the Head number/Sector Address from the data buffer prior to encountering each ID Field. Thus, by filling the data buffer with the desired Head Number/Sector Address information, the HDC can format an entire track with any given programmed sector interleave in one revolution.

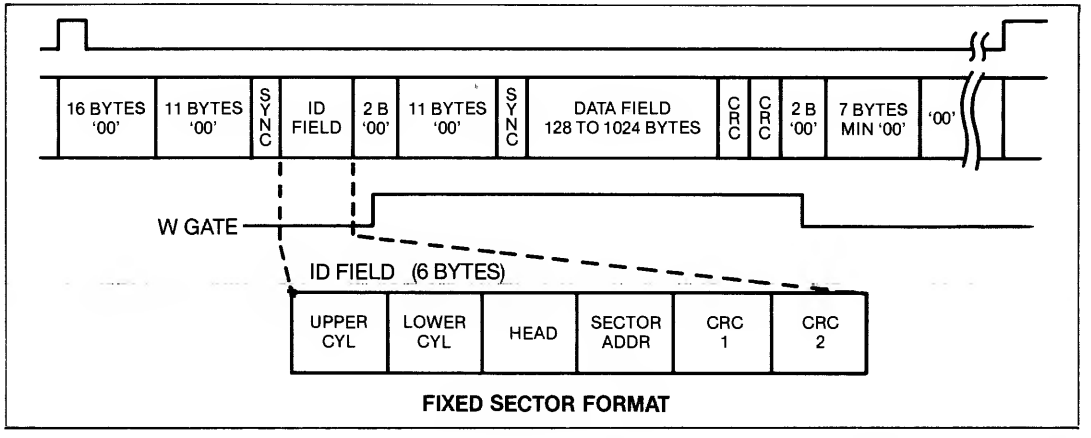
If the P flag is not set, the contents of the Sector Address field of the Task File will be incremented by one between sectors.

The $\overline{BCS}$ output will remain active for the duration of this command.

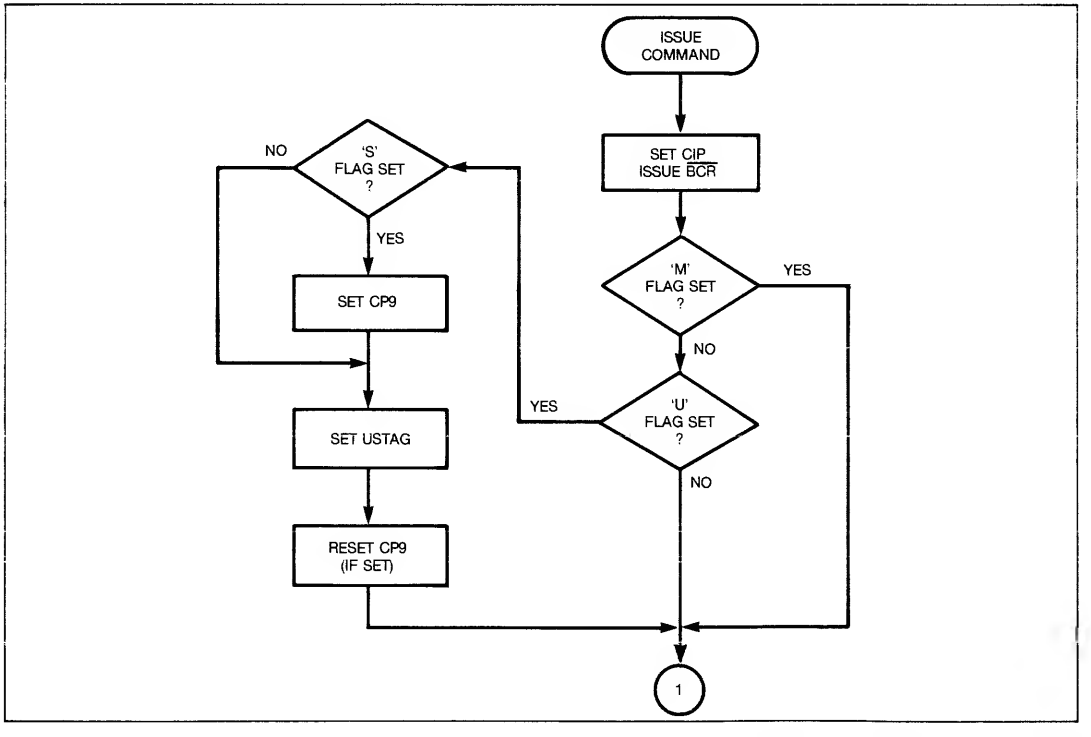
VERIFY SECTOR

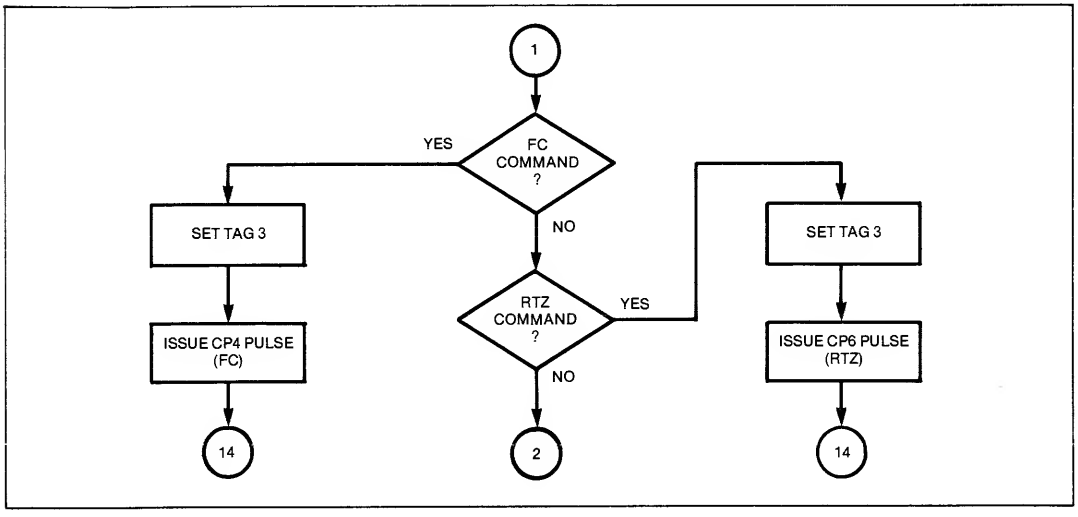
This command allows verification of sector format without transfer of data. Sector addressing is identical to that described for the Format Sector command. The IDNF, IDCE, DFNF and DFCE bits are set if errors are found (all bits are one's catching for multiple sector operation). With multiple sector operation, an entire track can be verified in a single revolution.

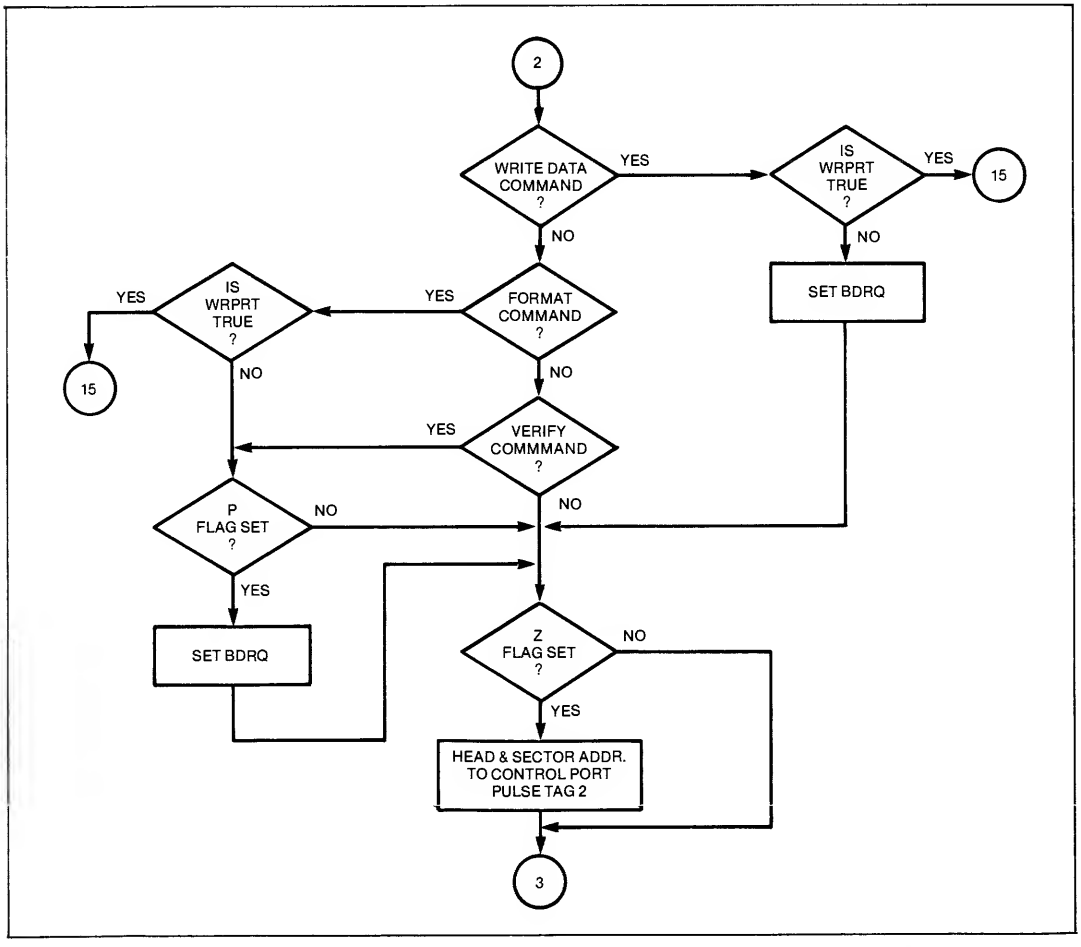
NOTE:
When used with the Lark drive, the validity of the DFCE bit is not guaranteed with this command if it immediately follows a FORMAT of the sector.

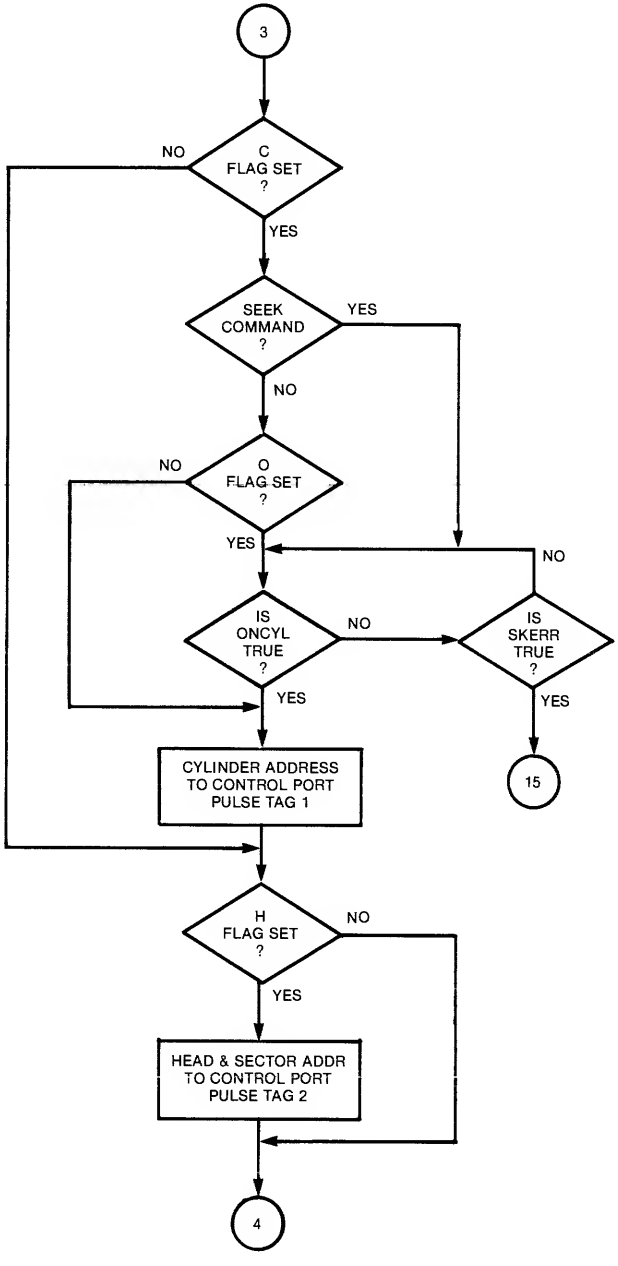


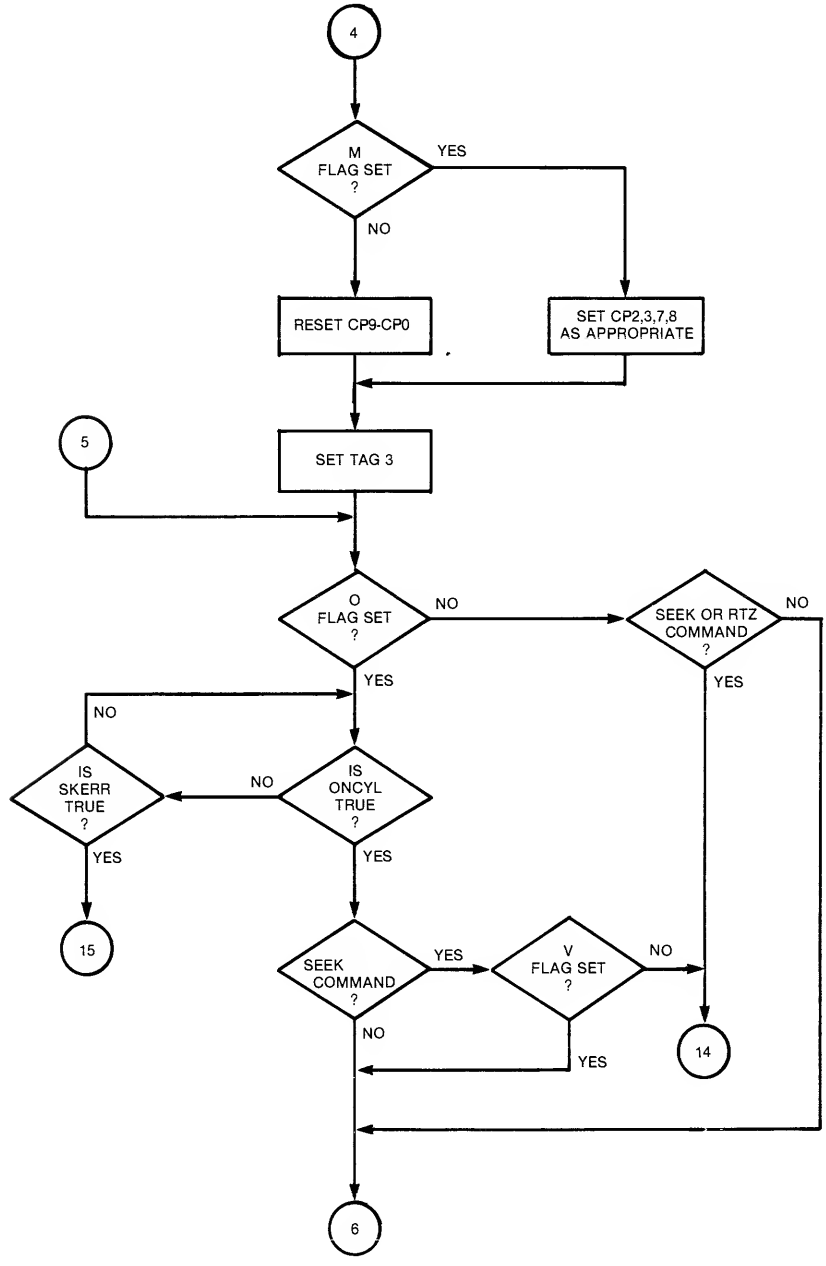
FIXED SECTOR FORMAT

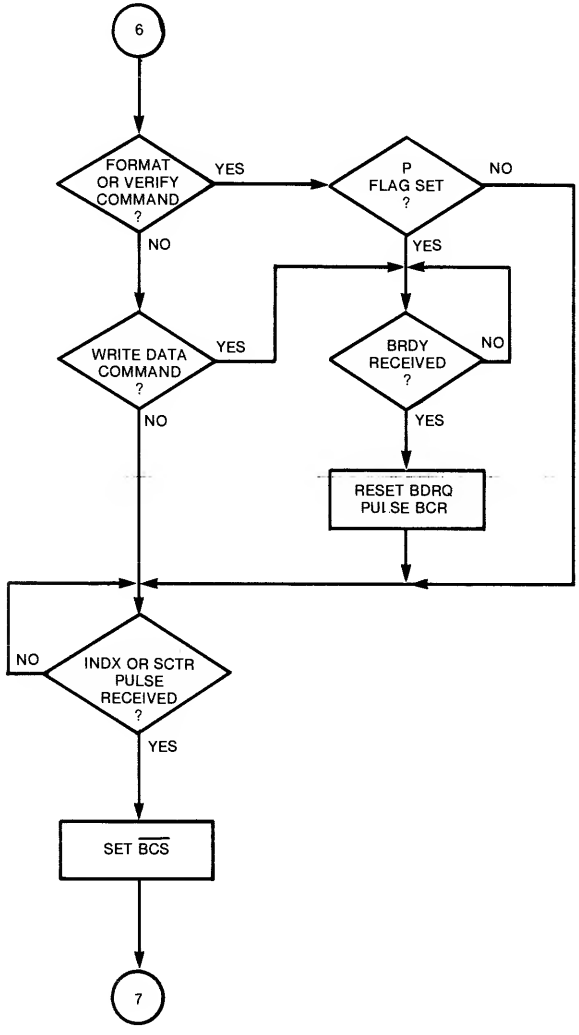


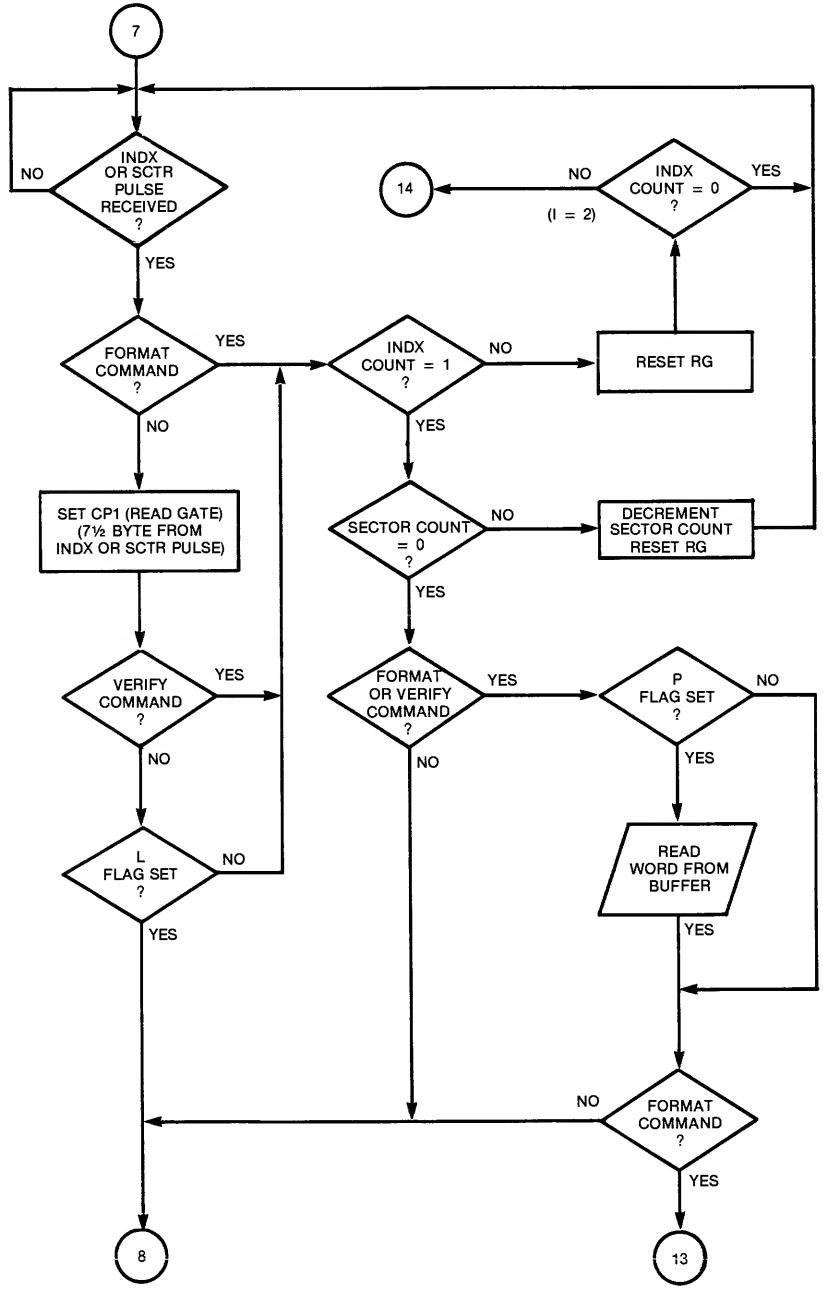

1
FC COMMAND ?
YES
NO
SET TAG 3
ISSUE CP4 PULSE (FC)
14
RTZ COMMAND ?
YES
NO
2
SET TAG 3
ISSUE CP6 PULSE (RTZ)
14

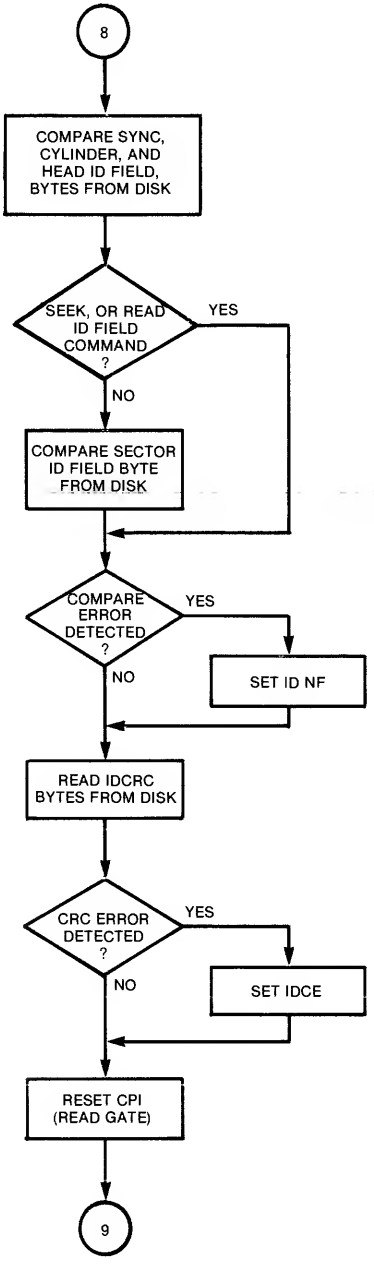

2
WRITE DATA COMMAND ?
YES
NO
IS WRPRT TRUE ?
YES
15
NO
SET BDRQ
FORMAT COMMAND ?
YES
NO
IS WRPRT TRUE ?
YES
15
NO
VERIFY COMMMAND ?
YES
NO
P FLAG SET ?
NO
YES
SET BDRQ
Z FLAG SET ?
NO
YES
HEAD & SECTOR ADDR. TO CONTROL PORT PULSE TAG 2
3

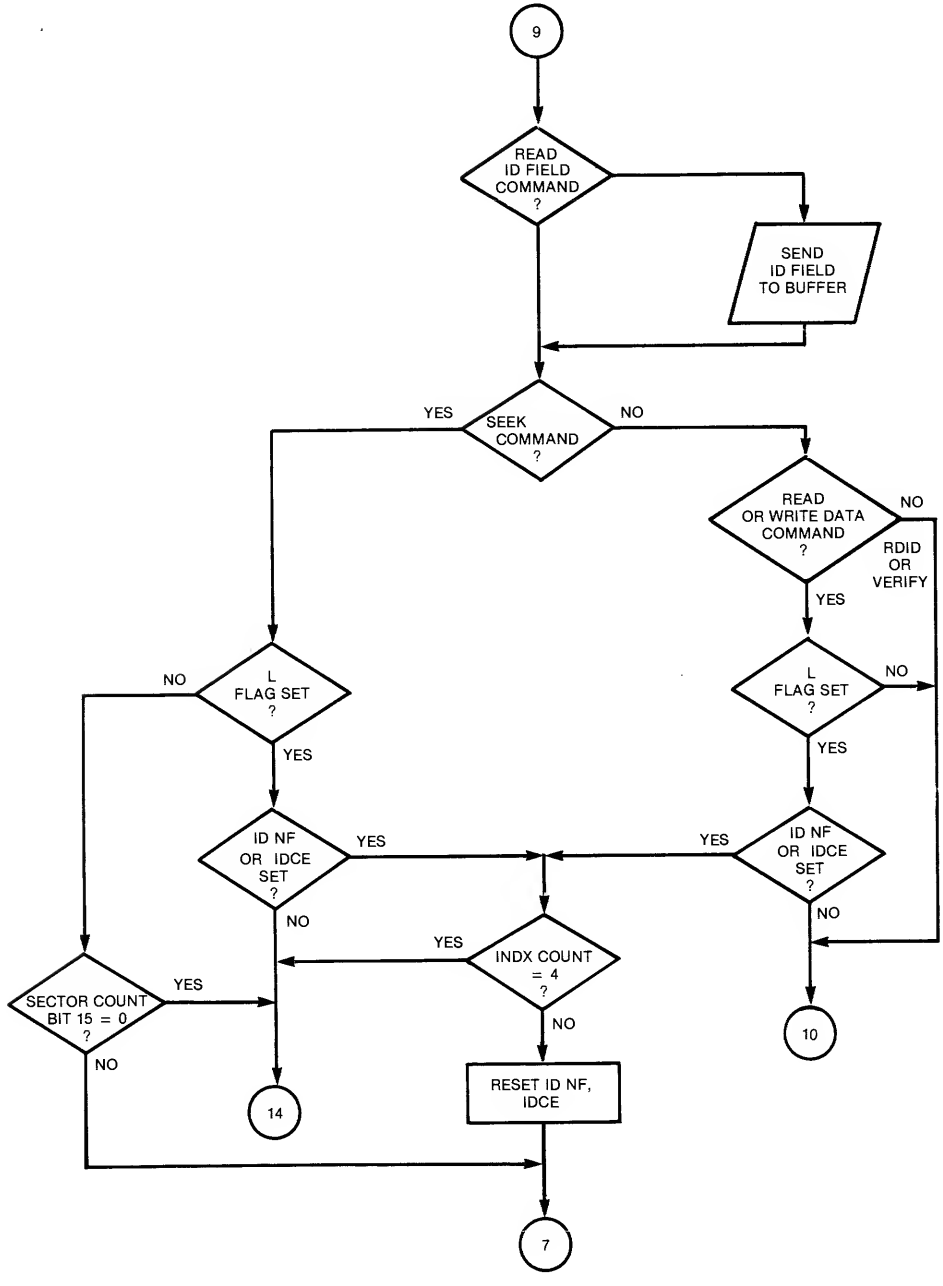

3
C FLAG SET ?
NO
YES
SEEK COMMAND ?
YES
NO
O FLAG SET ?
NO
YES
NO
IS ONCYL TRUE ?
NO
IS SKERR TRUE ?
YES
YES
CYLINDER ADDRESS TO CONTROL PORT PULSE TAG 1
15
H FLAG SET ?
NO
YES
HEAD & SECTOR ADDR TO CONTROL PORT PULSE TAG 2
4

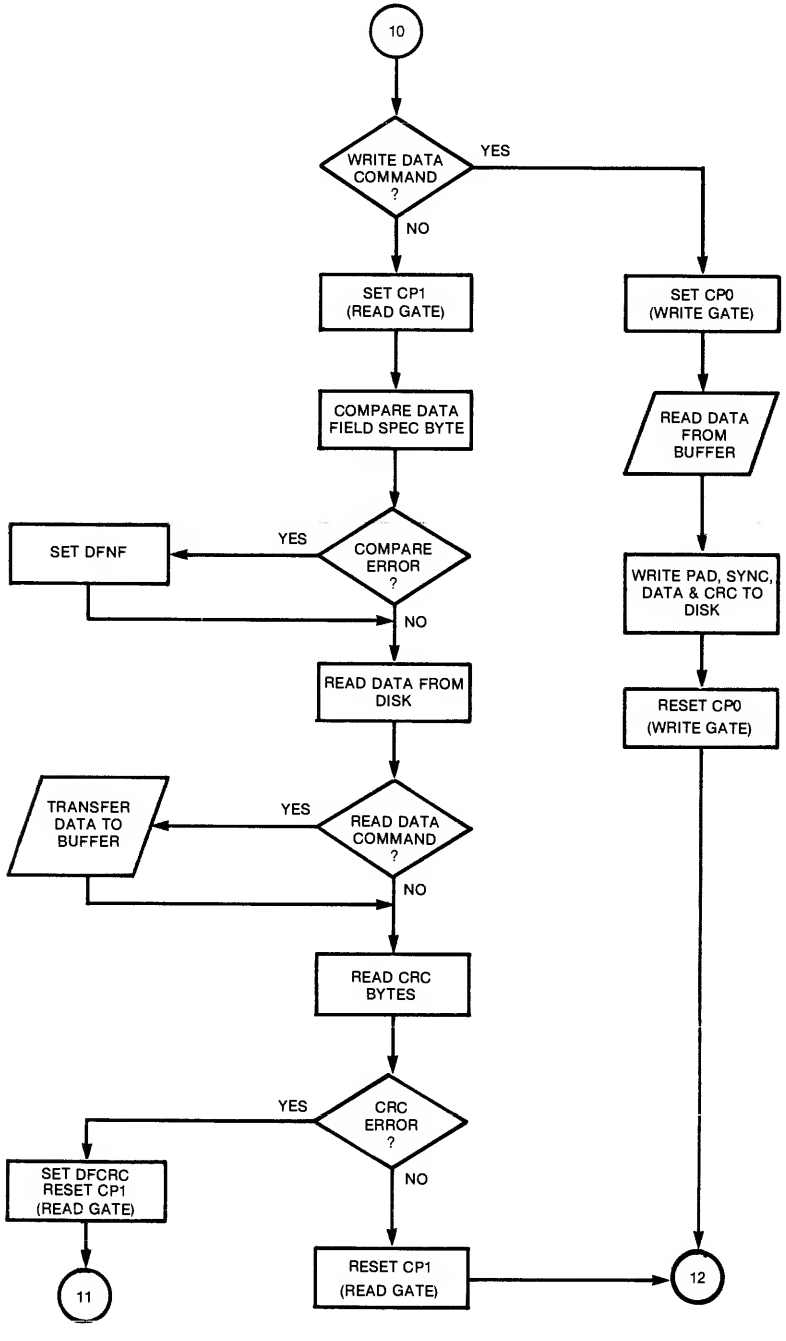

4
M FLAG SET ?
YES
NO
RESET CP9-CP0
SET CP2,3,7,8 AS APPROPRIATE
5
SET TAG 3
O FLAG SET ?
NO
SEEK OR RTZ COMMAND ?
NO
YES
YES
NO
IS SKERR TRUE ?
NO
IS ONCYL TRUE ?
YES
YES
15
SEEK COMMAND ?
YES
V FLAG SET ?
NO
NO
YES
14
6

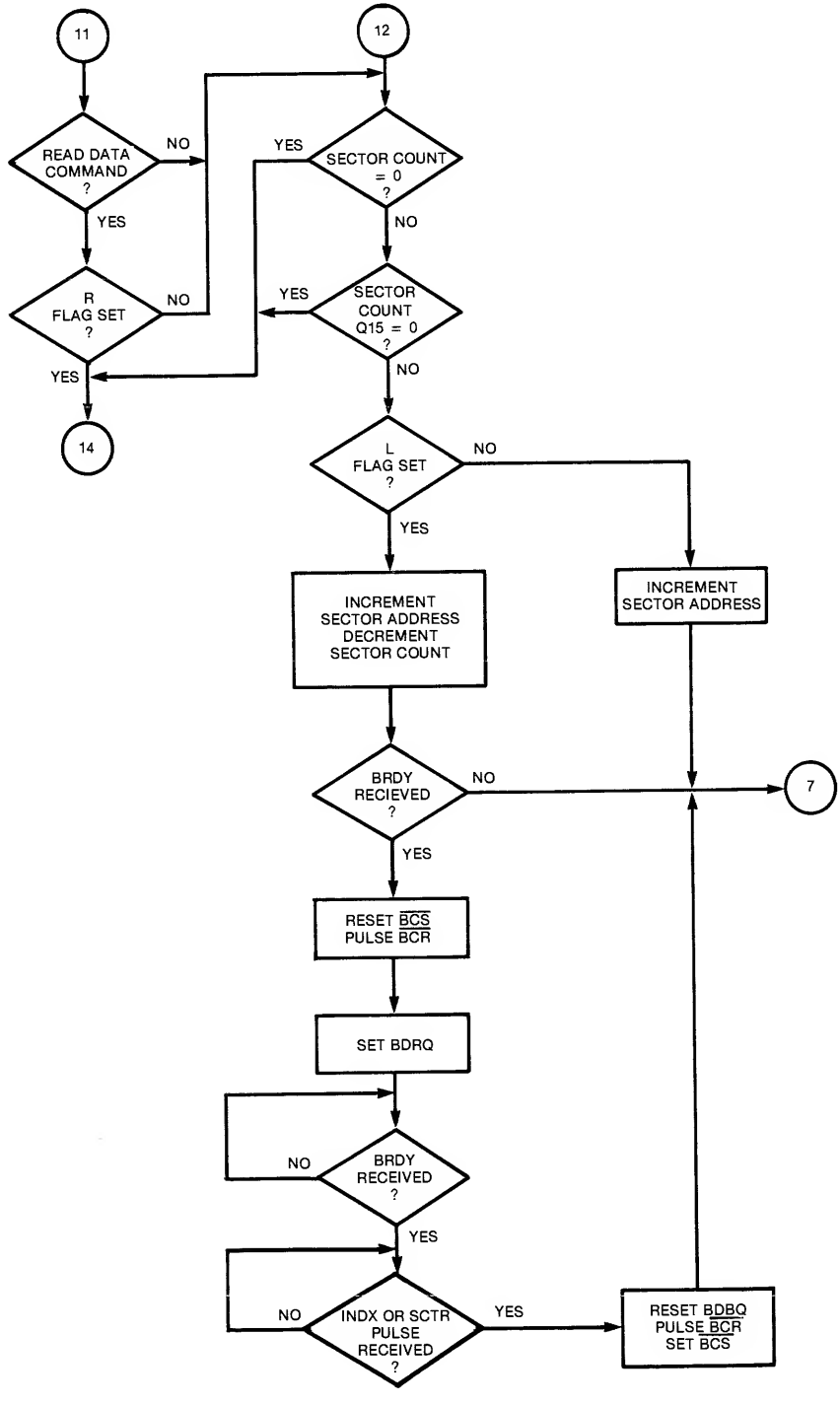

6
FORMAT OR VERIFY COMMAND ?
YES
NO
P FLAG SET ?
NO
YES
WRITE DATA COMMAND ?
YES
NO
BRDY RECEIVED ?
NO
YES
RESET BDRQ PULSE BCR
NO
INDX OR SCTR PULSE RECEIVED ?
YES
SET $\overline{BCS}$
7

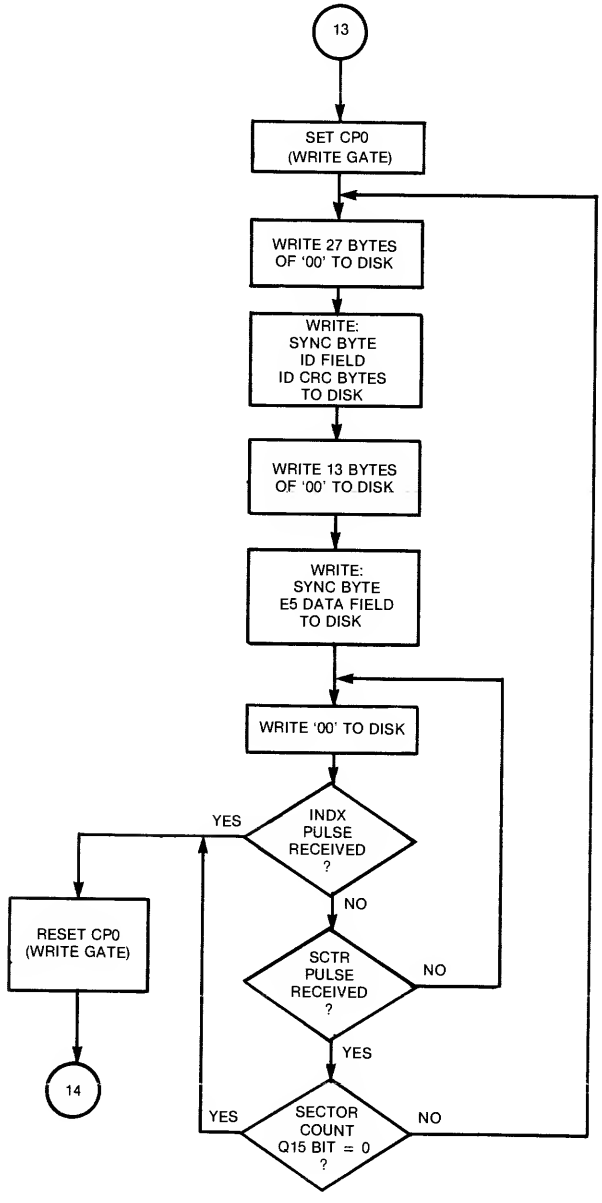

7
INDX OR SCTR PULSE RECEIVED ?
NO
YES
FORMAT COMMAND ?
YES
NO
INDX COUNT = 1 ?
NO
YES
RESET RG
SET CP1 (READ GATE) (7½ BYTE FROM INDX OR SCTR PULSE)
SECTOR COUNT = 0 ?
NO
YES
DECREMENT SECTOR COUNT RESET RG
VERIFY COMMAND ?
YES
NO
FORMAT OR VERIFY COMMAND ?
YES
NO
P FLAG SET ?
NO
YES
L FLAG SET ?
NO
YES
READ WORD FROM BUFFER
YES
FORMAT COMMAND ?
NO
YES
8
13
14
INDX COUNT = 0 ?
NO
(I = 2)
YES

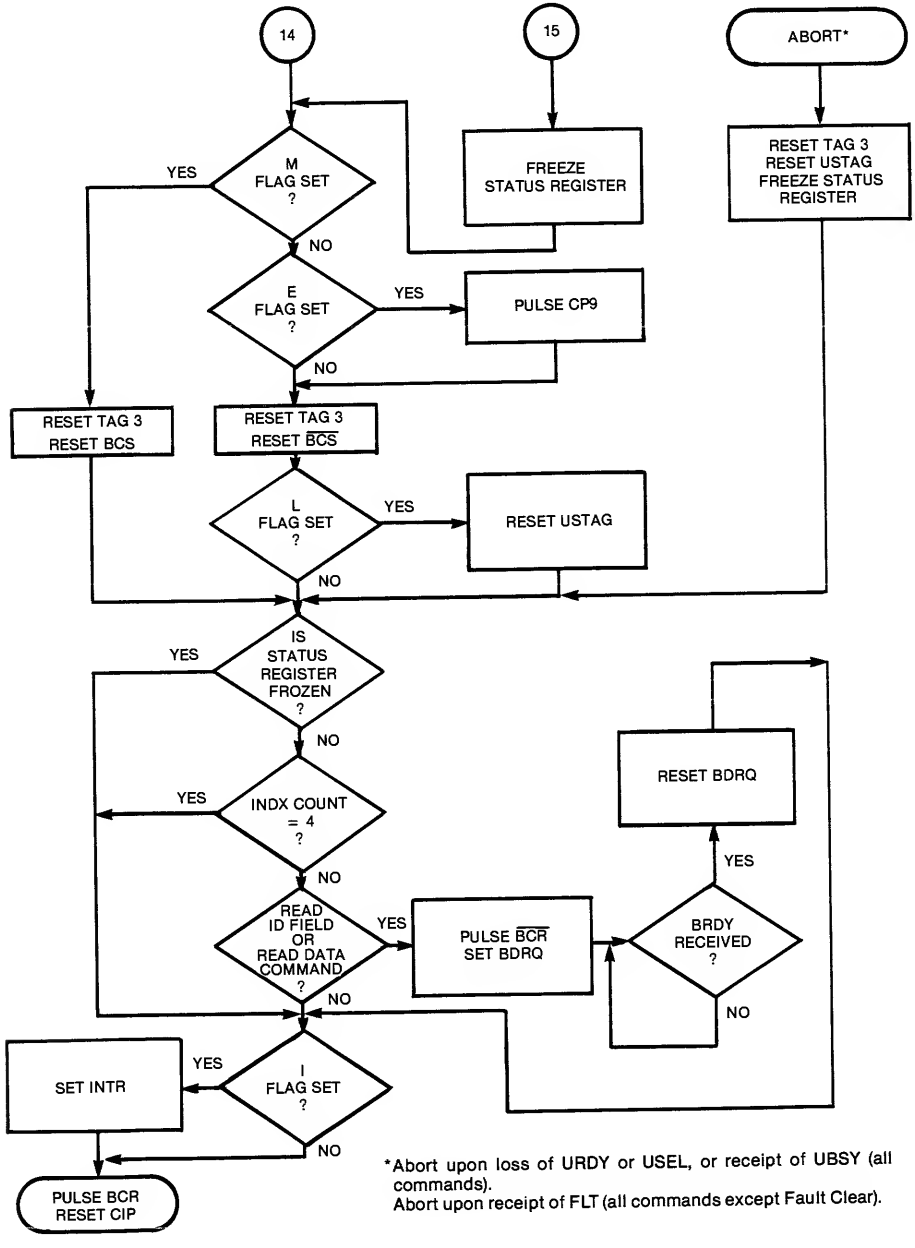

8
COMPARE SYNC, CYLINDER, AND HEAD ID FIELD, BYTES FROM DISK
SEEK, OR READ ID FIELD COMMAND ?
YES
NO
COMPARE SECTOR ID FIELD BYTE FROM DISK
COMPARE ERROR DETECTED ?
YES
NO
SET ID NF
READ IDCRC BYTES FROM DISK
CRC ERROR DETECTED ?
YES
NO
SET IDCE
RESET CPI (READ GATE)
9


9
READ ID FIELD COMMAND ?
SEND ID FIELD TO BUFFER
YES
SEEK COMMAND ?
NO
READ OR WRITE DATA COMMAND ?
NO
RDID OR VERIFY
YES
L FLAG SET ?
NO
YES
L FLAG SET ?
NO
YES
ID NF OR IDCE SET ?
YES
YES
ID NF OR IDCE SET ?
NO
NO
YES
INDX COUNT = 4 ?
SECTOR COUNT BIT 15 = 0 ?
YES
NO
NO
10
14
RESET ID NF, IDCE
7


10
WRITE DATA COMMAND ?
YES
NO
SET CP1 (READ GATE)
SET CP0 (WRITE GATE)
COMPARE DATA FIELD SPEC BYTE
READ DATA FROM BUFFER
SET DFNF
YES
COMPARE ERROR ?
WRITE PAD, SYNC, DATA & CRC TO DISK
NO
READ DATA FROM DISK
RESET CP0 (WRITE GATE)
TRANSFER DATA TO BUFFER
YES
READ DATA COMMAND ?
NO
READ CRC BYTES
YES
CRC ERROR ?
SET DFCRC RESET CP1 (READ GATE)
NO
RESET CP1 (READ GATE)
11
12


11
12
READ DATA COMMAND ?
NO
YES
SECTOR COUNT = 0 ?
YES
NO
R FLAG SET ?
NO
YES
SECTOR COUNT Q15 = 0 ?
YES
NO
14
L FLAG SET ?
NO
YES
INCREMENT SECTOR ADDRESS DECREMENT SECTOR COUNT
INCREMENT SECTOR ADDRESS
BRDY RECIEVED ?
NO
7
YES
RESET $\overline{BCS}$ PULSE $\overline{BCR}$
SET BDRQ
NO
BRDY RECEIVED ?
YES
NO
INDX OR SCTR PULSE RECEIVED ?
YES
RESET BDBQ PULSE $\overline{BCR}$ SET $\overline{BCS}$


13
SET CP0
(WRITE GATE)
WRITE 27 BYTES
OF '00' TO DISK
WRITE:
SYNC BYTE
ID FIELD
ID CRC BYTES
TO DISK
WRITE 13 BYTES
OF '00' TO DISK
WRITE:
SYNC BYTE
E5 DATA FIELD
TO DISK
WRITE '00' TO DISK
INDX
PULSE
RECEIVED
?
YES
NO
SCTR
PULSE
RECEIVED
?
NO
YES
SECTOR
COUNT
Q15 BIT = 0
?
YES
NO
RESET CP0
(WRITE GATE)
14



*Abort upon loss of URDY or USEL, or receipt of UBSY (all commands).
Abort upon receipt of FLT (all commands except Fault Clear).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

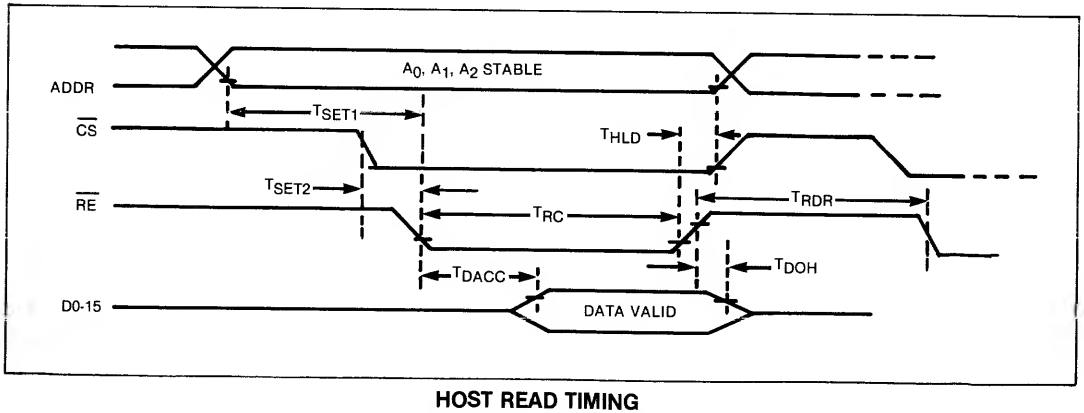
DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ±.25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = −100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	FOR PINS 25, 26, 27:				See Note 1
V_{IH}	Input High Voltage	V_{CC}		V	
V_{IL}	Input Low Voltage		V_{SS} + ⩽0.4 V	V	

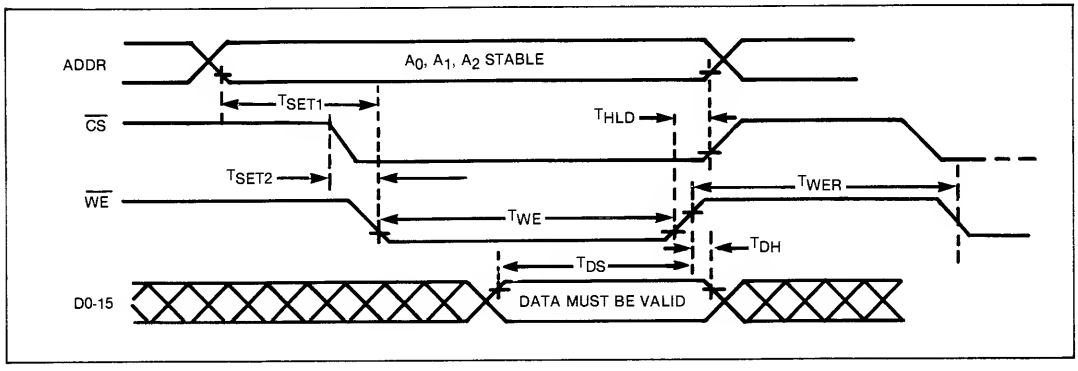
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ±.25V

HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SET1}	ADDR, Set up to $\overline{RE}$	80		nsec	
T_{SET2}	$\overline{CS}$ Set up to $\overline{RE}$	0		nsec	
T_{DACC}	Data Valid from $\overline{RE}$		375	nsec	C_L = 100 pF
T_{RC}	Read Enable Pulse Width	.375	5.0	μsec	
T_{DOH}	Data Hold from $\overline{RE}$		150	nsec	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		nsec	
T_{RDR}	Read Recovery Time	500		nsec	



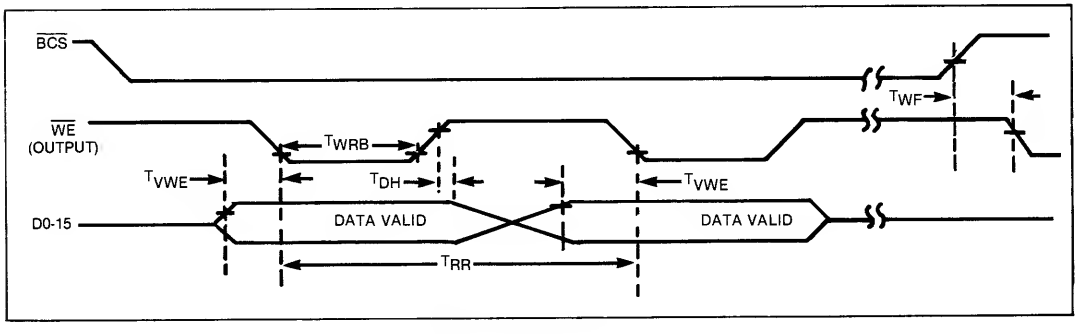
HOST READ TIMING



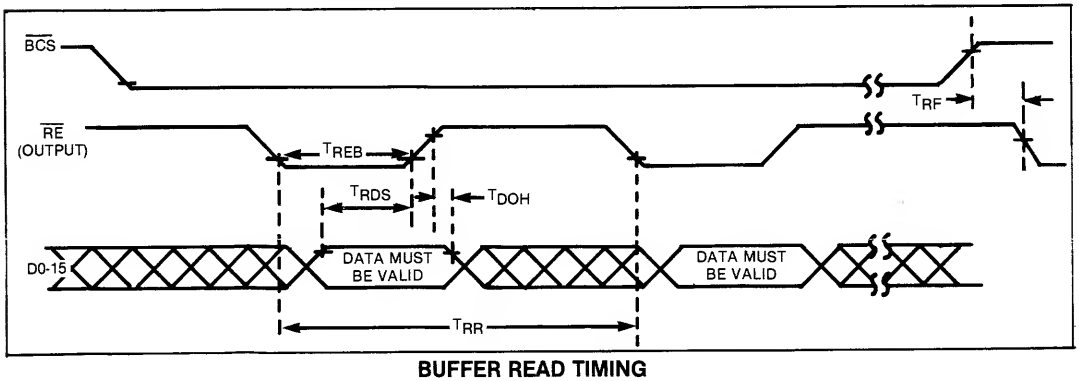
HOST WRITE TIMING

HOST WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SET1}	ADDR, Set up to $\overline{WE}$	80		nsec	
T_{SET2}	$\overline{CS}$ Set up to $\overline{WE}$	0		nsec	
T_{DS}	Data Bus Setup to $\overline{WE}$	100		nsec	
T_{WE}	Write Enable Pulse Width	200		nsec	
T_{DH}	Data Bus Hold from $\overline{WE}$	80		nsec	
T_{HLD}	ADDR, $\overline{CS}$ Hold from $\overline{WE}$	0		nsec	
T_{WER}	Write Recovery Time	1.0		μsec	



BUFFER WRITE TIMING



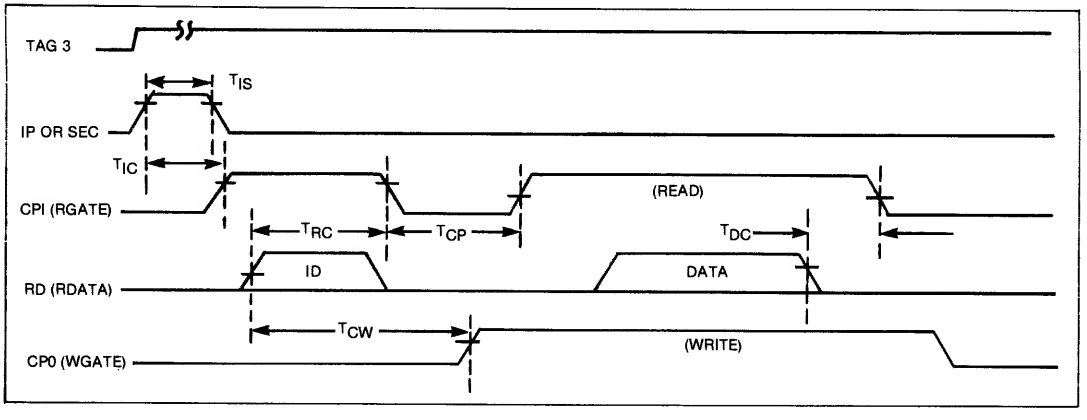
BUFFER READ TIMING

BUFFER WRITE TIMING (READ SECTOR CMD)

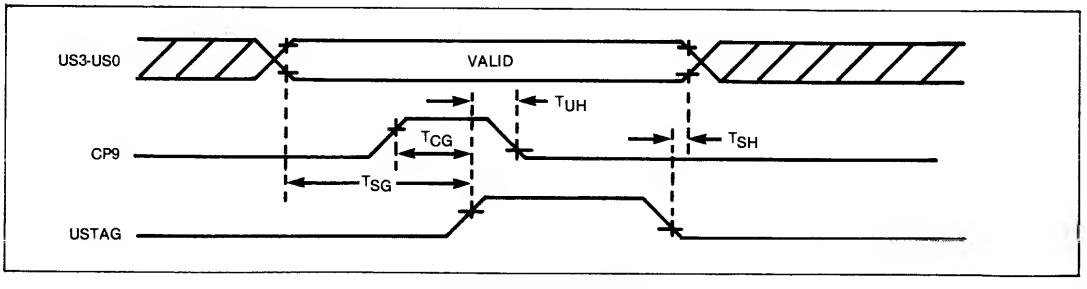
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WRB}	$\overline{WE}$ Output Pulse Width		4		SC	See Note 2
T_{VWE}	Data Set up to $\overline{WE}$		4		SC	See Note 2
T_{DH}	Data Hold from $\overline{WE}$		4		SC	See Note 2
T_{RR}	$\overline{WE}$ Repetition Rate		16		SC	See Note 2
T_{WF}	$\overline{WE}$ Float from $\overline{BCS}$			0	nsec	

BUFFER READ TIMING (WRITE SECTOR CMD)

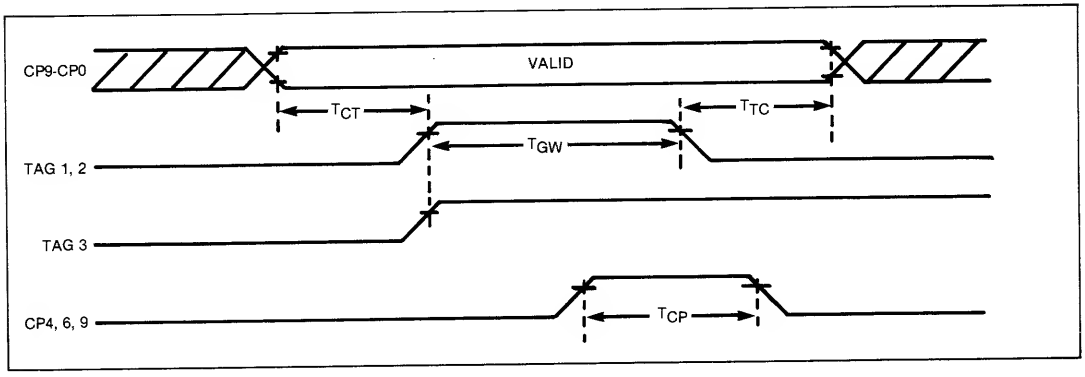
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REB}	$\overline{RE}$ Output Pulse Width		4		SC	See Note 2
T_{RDS}	Data Setup to $\overline{RE}$	100			nsec	
T_{RR}	$\overline{RE}$ Repetition Rate		16		SC	See Note 2
T_{DOH}	Data Hold from $\overline{RE}$	80			nsec	
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			0	nsec	



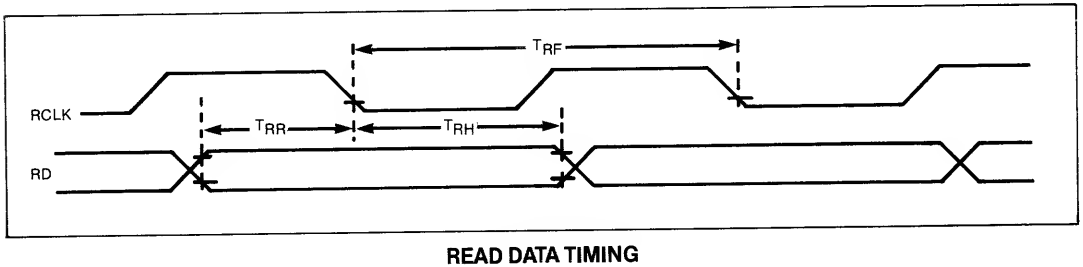
DISK R/W CONTROL TIMING



UNIT SELECT TIMING



CP TAG TIMING



READ DATA TIMING

DISK R/W CONTROL TIMING (SCLK = 9.677 MHZ)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{IS}	Index/Sector Pulse Width	.2	1.25	3.0	μsec	
T_{IC}	Index/Sector to CP1 High		60		SC	See Note 3
T_{RC}	CP1 Low from Read Data		56		SC	See Note 3
T_{CP}	CP1 Low to CP1 High			12	SC	See Note 3
T_{DC}	Last Read Data to CP1 Low		16		SC	See Note 3
T_{CW}	CP0 High from Read Data		60		SC	See Note 3

UNIT SELECT TIMING (SCLK = 9.677 MHZ)

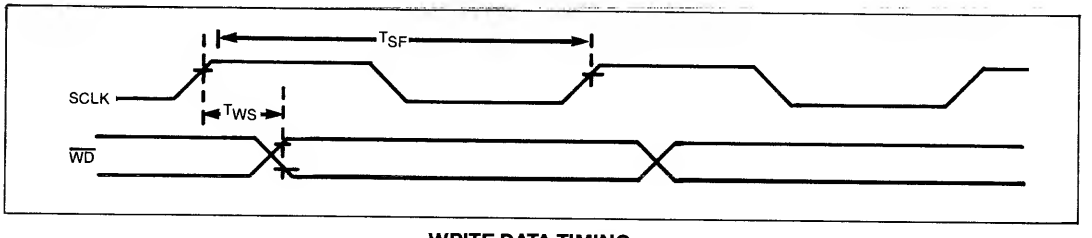
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{SG}	US3-US0 Setup to USTAG	2.0			μsec	
T_{CG}	CP9 Setup to USTAG		4		CLK	See Note 4
T_{UH}	CP9 Hold Time from USTAG		4		CLK	See Note 4
T_{SH}	US3-US0 Hold Time from USTAG	2.0			μsec	

CP TAG TIMING (SCLK = 9.677 MHZ)

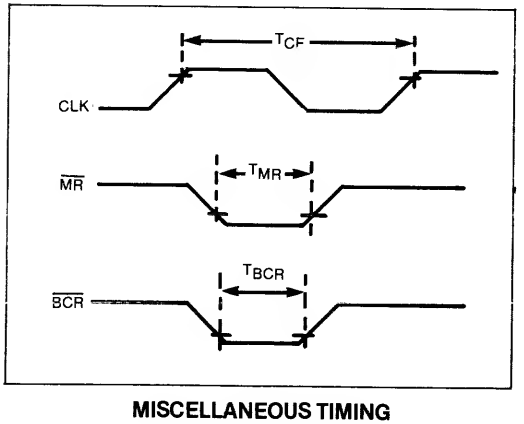
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{CT}	CP9-CP0 Setup to TAGS 1, 2, or 3		5		CLK	See Note 4
T_{GW}	TAGS 1 & 2 Pulse Width		4		CLK	See Note 4
T_{TC}	CP9-CP0 Hold Time from TAG 1, 2 Low		2		CLK	See Note 4
T_{CP}	CP4, 6, 9 Pulse Width During TAG 3 True		4		CLK	See Note 4

READ DATA TIMING

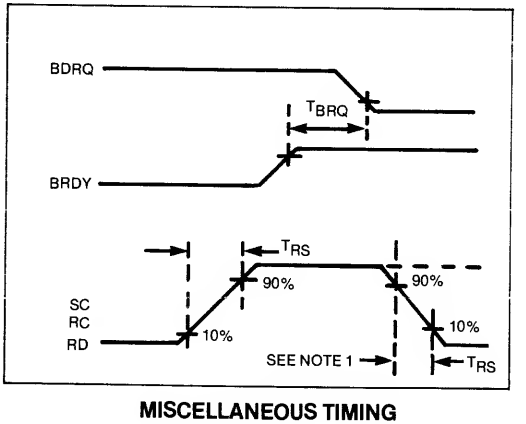
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RF}	RCLK Frequency	1.0	9.677	10.1	MHZ	
T_{RR}	Read Data Setup to RCLK Low	35			nsec	
T_{RH}	Read Data Hold Time from RCLK Low	0			nsec	



WRITE DATA TIMING



MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{SF}	Servo Clock Frequency	1.0	9.677	10.1	MHZ	
T_{WS}	$\overline{WD}$ Valid from Servo Clock High			85	nsec	C_L = 15 pf. See Note 5

MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{CF}	Master Clock Frequency		2.0	2.5	MHZ	50% Duty Cycle
T_{MR}	Master Reset Pulse Width	12			μsec	CLK Active
T_{BCR}	$\overline{BCR}$ Pulse Width		4		CLK	See Note 4
T_{BRQ}	BDRQ Reset from BRDY	50		600	nsec	
T_{RS}	Rise or Fall Time			15	nsec	See Note 1

NOTES:
1. It is recommended to buffer the line receiver stage with a TTL or Schottky TTL stage on pins 25, 26 and 27. A current sink capability of 48 mA with a 100 ohm pull-up resistor will provide both the required rise and fall times and also the required voltage swing. It is recommended to locate these buffers physically near the WD1050 to minimize inductive ringing.
2. Timing is a function of the Servo Clock (SCLK) frequency. The number of SCLK periods is specified. (Disregard "TYP" in this case.)
3. Timing is a function of the Servo Clock (SCLK) frequency. The number of negative SCLK transitions plus 400 nsec. max. is specified. (Disregard the "TYP" in this case.)
4. Timing is a function of the Master Clock (CLK) frequency. The number of CLK periods is specified. (Disregard the "TYP" in this case.)
5. $\overline{WD}$ is an open drain output and requires an external 1K ohm pull-up to V_{CC}. This pin is inverted relative to the SMD interface cable. It is recommended that this output go to the 'D' input of a 74S74 flip-flop that is clocked by the SCLK buffer described in Note 1. The 74S74 $\overline{Q}$ output may then connect to the interface line driver. It is recommended that the 74S74 be located physically near the WD1050.
6. All AC timing is measured at V_{OL} = 0.8 V, V_{OH} = 2.0 V.

See page 481 for ordering information.

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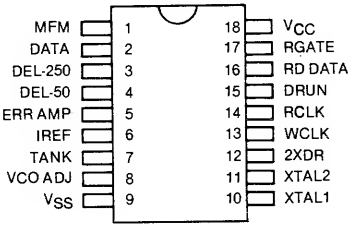
ADVANCED INFORMATION

WD1011 Winchester Data Separator Device

FEATURES

- 4.34 OR 5.0 MBIT/SEC DATA RATE
- SINGLE +5V SUPPLY
- FM OR MFM OPERATION
- COMPATIBLE WITH THE WD1010
- WRITE CLOCK GENERATOR
- HIGH FREQUENCY DETECTION



PIN DESIGNATION

DESCRIPTION

The WD1011 Winchester Data Separator has been designed to replace the complex analog/digital circuitry required for data recovery by Winchester disk drives. Directly interfacing to the WD1010 Winchester Controller device, the WD1011 allows operation of 4.34 Mbit/sec or 5.0 Mbit/sec transfer rates. In addition to data recovery, the device provides Write Clock signals for the WD1010 as well as high frequency detection for pre-amble search. Output levels on data pins swing close to the supply rails for increased noise immunity and to minimize layout restrictions.

The WD1011 operates from a single +5 volt supply and is available in an 18 pin plastic or ceramic Dual-in-Line package.

2.0.2 PIN DESIGNATIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	MFM	MFM	MFM read data input from the disk.
2	DATA	DATA	Output which extends width of disk pulse externally connected to input of delay element.
3	DELAY-250nSEC	DEL-250	Input to DRUN — externally connected to 250ns output of delay element.
4	DELAY-50nSEC	DEL-50	Input to phase detector and DRUN — externally connected to 50ns output of delay element.
5	ERROR AMPLIFIER	ERR AMP	Output from error amplifier — externally connected to input of low pass filter.
6	INPUT CURRENT REFERENCE	IREF	Input current reference used to stabilize error amplifier.
7	TANK	TANK	Variable capacitor is connected to this pin to adjust the open loop frequency of the VCO.
8	VCO ADJUSTMENT	VCO ADJ	Input to VCO TANK — externally connected to output of low pass filter.
9	V_{SS}	V_{SS}	Ground.
10	XTAL1	XTAL1	Crystal oscillator connection, or connection to TTL driver.
11	XTAL2	XTAL2	Crystal oscillator connection, or no connection if external TTL driver is used.
12	DATA REFERENCE CLOCK	2XDR	Data Reference clock.
13	WRITE CLOCK	WCLK	Write Clock output. (Frequency = RCLK)
14	READ CLOCK	RCLK	Read Clock synchronous with MFM data read from the disk.
15	DRUN	DRUN	DRUN output signal that is true whenever there is a continuous stream of either MFM ones or zeros.
16	READ DATA	RDDATA	Output of disk pulse extended MFM bits — externally connected to WD2183.
17	READ GATE	RGATE	Read Gate input from the WD2183 used to multiplex the reference clock or MFM to the phase comparator: If RGATE = 0 reference is enabled If RGATE = 1 MFM is enabled
18	V_{CC}	V_{CC}	+5V ± 5% Substrate.

See page 481 for ordering information.

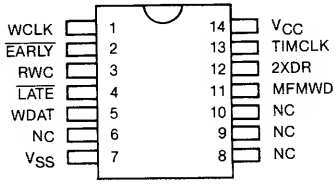
Printed in U.S.A

ADVANCED INFORMATION

WD1012 Write Precompensation Device

FEATURES

- INTERNAL DELAY LINE
- COMPATIBLE WITH THE WD1010
- INTERFACES DIRECTLY WITH TTL LOGIC
- CMOS TECHNOLOGY
- SINGLE +5VDC SUPPLY
- USED WITH SHUGART SA1000, SEAGATE TECHNOLOGY ST506, AND OTHER COMPATIBLE DRIVES



PIN DESIGNATION

DESCRIPTION

The WD1012 Write Precompensation Logic Device has been designed to replace a complexity of logic circuitry as well as several TTL packages. By designing the Write Precomp delay line into the package, an additional device is replaced reducing on-board space and design requirements and minimizing layout restrictions.

The WD1012 is designed to be used with the WD1010 for Winchester disk operation. The WD1012 operates from a single +5VDC supply and is manufactured using CMOS technology. The device is available in a 14 pin, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	SIGNAL	SIGNAL NAME	DESCRIPTION
1	WCLK	WRITE CLOCK	Write Clock input required to generate TIMCLK output.
2	$\overline{\text{EARLY}}$	$\overline{\text{EARLY}}$	Input from WD1010 used to gate internal Time Delay (EP) to WDAT output.
3	RWC	REDUCE WRITE CURRENT	Reduce Write Current input from the WD1010. When RWC is low, NOMINAL is high. If RWC is high and either EARLY or LATE is enabled to the WDAT multiplexer then NOMINAL is disabled, otherwise it is high. Both EARLY and LATE cannot be active at the same time.
4	$\overline{\text{LATE}}$	$\overline{\text{LATE}}$	Input from WD1010 used to gate internal time delay (LD) to WDAT output.
5	WDAT	WRITE DATA	This output line to the disk is multiplexed to the internal delay line taps (ED, ND, LD) using gated signals $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$ respectively.
6	NC	NO CONNECTION	
7	V_{SS}	GROUND	Ground.
8-10	NC	NO CONNECTION	
11	MFMWD	MFM WRITE DATA	MFM Write Data input from the WD1010. This signal is latched with 2XDR internally and transmitted to the external delay line on DOUT.
12	2XDR	2X DATA REFERENCE	This input reference clock latches MFMWD internally.
13	TIMCLK	TIMING CLOCK	Timing Clock output used by the SA1000 drives as a stepping rate reference in the stepper control circuitry. WCLK is divided down by 16 to produce TIMCLK.
14	V_{CC}	+5VDC	+5VDC input supply.

See page 481 for ordering information.

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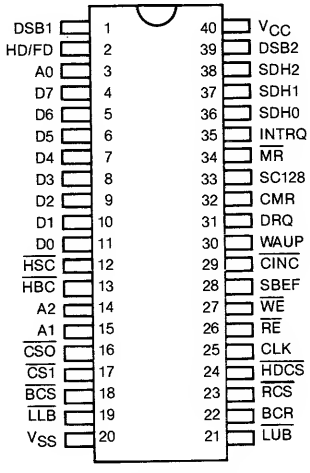
PRELIMINARY

WD1014 Error Detection/Support Logic Device

FEATURES

- 32 BIT ECC POLYNOMINAL
- BURST CORRECTION TO 5 BITS
- MULTIPLE ERROR BURST DETECTION
- DATA TRANSFER RATE OF 5 M BITS/SECOND
- PROCESSES CHECK/SYNDROME BITS IN 2-BIT SERIAL FASHION
- SECTOR SIZES = 128, 256, 512, & 1024 BYTE DATA FIELDS
- SUPPORT READ/WRITE SHORT/LONG FEATURES
- ON-CHIP STORAGE OF SYNDROME/CHECK BYTES
- 8-BIT I/O DATA BUS
- SOFTWARE ADDRESSABLE REGISTERS & LATCHES
- ON-CHIP LOGIC FOR EXTERNAL BUFFER CONTROL
- 40-PIN, DUAL-IN-LINE, N-MOS DEVICE
- TTL, MOS COMPATABILITY
- SINGLE SOURCE +5 VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1014 EDS logic chip provides the WD1002-05 Winchester Floppy Disk Controller (WFC) board with ECC and support logic. The EDS chip is a single chip device specifically designed to add error correction capabilities to a 5.25" Winchester disk drive. It also contains three 8-bit registers, three counters, and several latches that enhance the capability of the WFC on-board Control Processor (CP) chip WD1015) for control functions in real time operation. The EDS 40-pin device replaces approximately 35 standard TTL packages consisting of shift registers, flip-flops, and logic gates.

The ECC polynomial selected is the same as the one implemented in the WD1100-06 ECC/CRC logic except that the current design is a 2-bit serial implementation of the polynomial for faster operation. The ECC polynomial selected is a computer generated code optimized for sector sizes of 128, 256, 512, and 1024 byte data fields. The four ECC bytes appended by this chip enable correction of a single burst of up to 5 bits. It can also a single burst of up to 20 bits and a double burst of up to 4 bits. The computer generated code has been selected over a comparable fire code since fire codes suffer from a pattern sensitivity problem.

The WD1014 EDS device is fabricated using N-channel silicone gate technology, and is available in a 40-pin, ceramic, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1 39	DRIVE SELECT BIT 2 DRIVE SELECT BIT 2	DSB1 DSB2	These two output lines are encoded to select one of three Winchester Drives or one of four floppy drives depending upon the state of HD/$\overline{FD}$.
2	HARD OR FLOPPY DISK SELECT	HD/$\overline{FD}$	When high hard disk drives are selected and when low floppy disk drives are selected.
3 14 15	ADDRESS BIT 0 ADDRESS BIT 2 ADDRESS BIT 1	A0 A2 A1	These 3 input lines along with $\overline{CS0}$, $\overline{CS1}$, are used to address the interim registers.
16 17	CHIP SELECT BIT 0 CHIP SELECT BIT 1	$\overline{CS0}$ $\overline{CS1}$	One of these 2 lines should be low to select the registers as shown under task files.
4-11	DATA BUS	D7-D0	8 bit bidirectional data bus. Data is output only when the check/syndrome register or the command register is read.
12	HOST STATUS CONTROL	$\overline{HSC}$	This output when low, enables the WFC status onto the data lines available to the host processor.
13	HOST BUS CONTROL	$\overline{HBC}$	This output when low, enables the host to communicate to the WFC and set up all task files.
18	BUFFER CHIP SELECT	$\overline{BCS}$	This input line indicates that an external device wants to access the buffer. The ECC check/syndrome computation is also enabled at this time.
19	LOAD LOWER BYTE	$\overline{LLB}$	The rising edge of this output line is used to load the lower byte of address into the external buffer counter.
20	GROUND	V_{SS}	Ground.
21	LOAD UPPER BYTE	$\overline{LUB}$	The rising edge of this output line is used to load the upper byte of address into the external buffer counter.
22	BUFFER COUNTER RST.	BCR	This input indicates that an external device wants to reset the external buffer counters. The internal overflow counters are also cleared.
23	RAM CHIP SELECT	$\overline{RCS}$	This output line is used to select external RAM when $\overline{BCS}$ is active low or when the CP or the host is accessing the RAM.
24	HARD DISK CHIP SELECT	$\overline{HDCS}$	This output line is used to enable the WD1010 when the host is accessing its task files except the Error, Status and Command registers.
25	CLOCK	CLK	The rising edge of CLK is used to shift the ECC polynominal and the falling edge is used to count exactly 4 shifts.
26 27	READ ENABLE WRITE ENABLE	$\overline{RE}$ $\overline{WE}$	Strobes used in conjunction with $\overline{CS0}$, $\overline{CS1}$, AS-A0 to access registers.
28	SECTOR BUFFER EMPTY OR FULL	SBEF	Output signal used to indicate the sector buffer has been filled or emptied.
29	COUNTER INCREMENT	$\overline{CINC}$	The rising edge of this output signal increments an external address counter.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
30	WAKE UP	WAUP	This output signal is used to indicate that a command is being executed by the CP of the WFC board. The host cannot communicate with the WFC at this time until after the command has been completed.
31	DATA REQUEST	DRQ	The data request line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the sector buffer has been filled or emptied.
32	COUNTER MASTER RESET	CMR	This output signal resets the external address counters whenever a $\overline{MR}$ or a command has been issued by the host.
33	SECTOR COUNT OF 128 BYTES	SC128	This input signal is used in conjunction with the SDH register to indicate that the buffer has overflowed.
34	MASTER RESET	$\overline{MR}$	Used to initialize internal logic. All internal buffer overflow counters are reset, the DRQ and INTRQ flip-flops are cleared and BUSY is set.
35	INTERRUPT REQUEST	INTRQ	This output line is activated whenever a command has been completed. It is reset to the inactive state when the status register is read, or a new command is loaded via the DAL lines, or $\overline{MR}$ is asserted.
36 37 38	SECTOR SIZE DRIVE SELECT, AND HEAD SELECT BITS	SDH0 SDH1 SDH2	The least 3 significant bits of the internal SDH register are available as outputs. The SDH register is updated whenever the host writes to it.
40	+5 V	V_{CC}	+5 V input supply.

TASK FILES

WAKE UP, CS1, CS0, A2-A0, $\overline{RE}$ and $\overline{WE}$ are used to select various registers as shown below:

BUSY	CS1 –	CS0 –	A2-A0	EFFECT
X	1	1	X	Idle — Nothing selected.
0	1	0	X	Host to WFC and WD1010 files.
1	1	0	X	CP to WD1010 + RAM access.
1	0	1	X	CP to EDS registers.
X	0	0	X	Illegal condition.

			WD1010 REGISTERS		EDS REGISTERS	
A2	A1	A0	$\overline{RE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WD}$
0	0	0	RAM	RAM	0 + CHECK/SYN bytes	0 + CHECK bytes
0	0	1	Error Req.	Write Precomp		Set ECC
0	1	0	Sector Count	Sector Count	SLEEP	0 + LLB
0	1	1	Sector Number	Sector Number	Clear OVF/CNTRS	0 + LUB
1	0	0	Cylinder Low	Cylinder Low		Set DRQ
1	0	1	Cylinder High	Cylinder High		Set Read Latch
1	1	0	S.D.H.	S.D.H.	Clear Mult Mode	Set Mult Mode
1	1	1	Status Reg.	Command Reg.	0 + Command	0 + Error Reg.

COMMAND CODES

For the implementation of parts of the controls, the following command codes are pertinent:

COMMAND	BITS 7	6	5	4	3	2	1	0
READ	0	0	1	0	D	M	L	0
WRITE	0	0	1	1	0	M	L	0
FORMAT	0	1	0	1	0	0	0	0

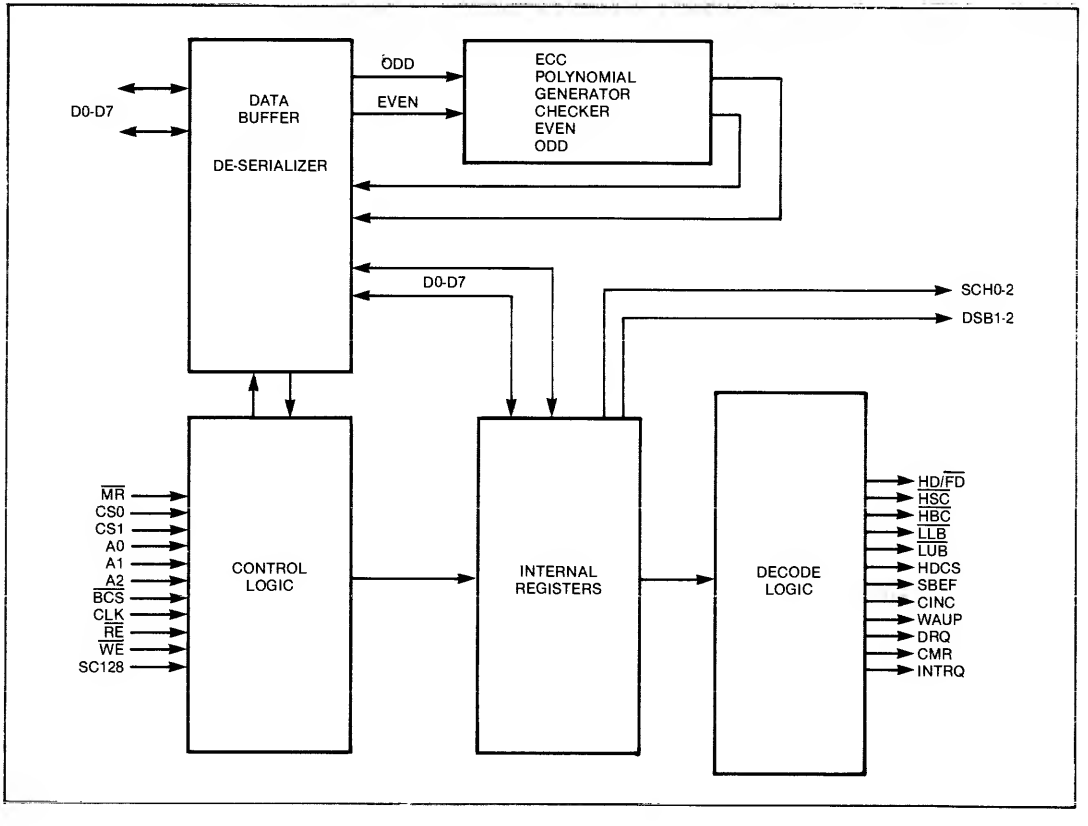
The control logic only decodes bits 7-4 and uses bit 1 (long bit) in its internal logic. The rest of the command codes and bits are not used by the EDS.

For a complete description of the commands or the task files refer to the WD1002-05 WFC data sheet.

WD1014 ARCHITECTURE

The WD1014 chip was specifically designed for the WFC board to extend the capabilities of the Control Processor (WD1015) to handle real time functions. As designed, the WD1014 is not a stand alone general purpose device unless, of course, almost all of the protocol described can be used in any new designs.

The WD1014 consists of a 2 bit serial polynomial generator (that produces 4 bytes of check/syndrome) an 8 bit data buffer and deserializer, two 8 bit latches, namely a Command/Error register and a SDH latch, and control logic consisting of 3 counters, 6 latches, and a host of combinatorial logic. The addressable registers and latches are accessed as shown in the block diagram below.



WD1014 BLOCK DIAGRAM

Each major functional block will be described essentially independent of one another. Some overlap and references to the WFC board are unavoidable and, in fact, they aid in presenting a clearer picture of the device.

THE ECC POLYNOMIAL GENERATOR

The 4 byte check/syndrome generator consists of two 16 bit shift registers each of which has 8 feedback terms implemented with XOR gates, and control gates for the feedback and data paths.

ECC computations are made whenever the external sector buffer is being accessed. The data present on the system data bus is accepted by the input data buffer and processed along with the gated data from the last stages of the shift register strings. The direction of shift within the ECC polynomial is from the L.S.B. to the M.S.B. After the last byte of data has been accessed from the sector buffer, the internal counter overflow register is set. This in turn sets a feedback inhibit register after the last byte has been processed by the ECC polynomial. At this point, the feedback terms are forced to zero and only the data path to the L.S.B. is enabled. This feature is convenient to store the 4 check/syndrome bytes internally so that RLONG and WLONG commands can be supported without the use of an external buffer.

During a write operation, the input data stream is divided by the polynomial and the 32 bit remainder obtained after buffer overflow is used as the 4 check bytes. The 4 check bytes are gated out of the WD1014 even though $\overline{RCS}$ = 1 since the internal $\overline{RBCS}$ is still active. In a READ operation, the check bytes are recomputed and compared to the recorded check bytes to generate the 4 syndrome bytes. The syndrome bytes are stored internally in the shift registers until the CP is ready to use them. Otherwise, the non-zero syndrome is used by the software algorithm to compute the displacement and the error vector within the bad sector.

To support RLONG and WLONG (L = 1) features of the WD1002-05, shift register strings are used as storage elements. After the last byte of data, the host can write or read the 4 additional bytes which serve as check bytes for the data transmitted to the buffer. In this mode the feedback terms and the outputs from M.S.B. of the shift registers are disabled so that only data is accepted and stored. This enables the user to alter the check bits/or data to verify the operation of the Error detection logic.

SDH REGISTER

This register can be written into by either the host or the CP. Bits 6 and 5 (sector size selection) are decoded as follows:

SDH6	SDH5	SECTOR SIZE IN BYTES
1	1	128
0	0	256
0	1	512
1	0	1024

The decoded bits are used in conjunction with a 3 bit counter which has SC128 as its clock. The falling edge of this input is used to set a counter overflow latch for sector sizes 256, 512 and 1024. The rising edge of this input sets counter overflow latch when the sector size is 128. The counter overflow is available on the output as SBEF and is used internally to set the buffer overflow latch and various other control logic as required by system operation. This counter and associated logic is cleared upon $\overline{MR}$, any new command, or can be directly cleared by CLROVF.

Bits 1-4 are encoded as follows:

$\overline{FD}$ = SDH4. SDH3
HD = $\overline{SDH4}$. $\overline{SDH3}$ = $\overline{SDH4}$ + $\overline{SDH3}$

	DSB2	DSB1
$\overline{FD}$/HD = 1	$\overline{SDH4}$	$\overline{SDH3}$
$\overline{FD}$/HD = 0	SDH2	SDH1

In addition, the latched bits 0, 1 and 2 are directly available as outputs.

COMMAND/ERROR REGISTER

This 8 bit register intercepts and holds the command issued by the host. When a command is issued:

(a) the sector counter and associated overflow latches are cleared

(b) the external counters are cleared via CMR

(c) the read command latch is cleared

(d) INTRQ is reset

(e) bit 1 (the long bit) is used by the ECC polynomial to implement the READLONG and WRITE LONG command. The CP can also read this latch so that it can execute the command.

(f) WAKEUP is set immediately if the command is a RESTORE, SEEK, or READ. For a WRITE or a FORMAT command, WAUP is set after counter overflow (COVF) occurs or an additional four RAM accesses have occured (SYN4), depending upon the long bit L = 0 or L = 1.

At the completion of a command, this register is reused to hold error information that can be read by the host. This is necessary since error information from 2 sources has to be manipulated by the CP and reported to the host in real time when requested to do so.

ERROR DETECTION LOGIC

The error detection logic consists of an input data buffer and deserializer, two 16 bit shift registers to generate the ECC bytes, and associated control logic consisting of two 3 bit counters and integrated logic.

INPUT DATA BUFFER AND DESERIALIZER

This section is designed to accept a byte of data on the rising edge of $\overline{RE}$ or $\overline{WE}$ under the following conditions:

1. The ECC polynomial is selected as implied by SDH7 = 1.
2. A valid $\overline{RBCS}$ is generated regardless of the counter overflow
3. If the syndrome is to be read by the C.P. after an overflow condition has occurred (i.e., the syndrome is not saved after it has been read by the C.P.).

Valid data presented to the WD1014 device is accepted by the data buffer and the ECC shift registers on the rising edge of RE or We input strobes. These strobes are synchronized internally by the falling edge of the input clock so that shifting can begin on the rising edge of the clock. Data is serialized and shifted in a 2 bit parallel mode until the internal bit counter reaches the count of 3. This process is repeated for every byte of data until the counter overflow occurs plus an additional 4 bytes have been processed. Under the worst case conditions, a byte of data will be processed within 4 clock cycles after the $\overline{RE}$ or $\overline{WE}$ strobes are terminated.

MULTIPLEXER

The multiplexer is used to channel data to the I/O pins D7-D0 when one of the following conditions occur.

1. The command register is read
2. The error register is read
3. The check bytes are read
4. The syndrome bytes are read

CONTROL LOGIC

This section will cover the rest of the control logic required for system operation not described as part of the other sections, in terms of the output signals.

WAKEUP

This signal alerts the external CP that a command has been received and is internally referred to as the busy signal.

This line is set high whenever $\overline{MR}$ is asserted or a command has been received unless it is a WRITE or a FORMAT command. In that case, WAUP is not set until SBEF = 1 (COVF) if L = 0, or until an additional 4 bytes have been accepted by the EDS if L = 1.

For proper operation, the READ command latch must be set by the CP whenever that command has been received. Also the Multiple Mode latch is set by the CP in order to execute the same command a multiple number of times. This latch must be reset if executing a READ or a WRITE command only once, or if the last sector of a multiple sector transfer is being processed.

WAKEUP can only be reset by asserting SLEEP.

DATA REQUEST

The true condition of the DRQ latch can only be sampled by external circuitry if WAUP = 0.

This latch can be set by either the CP, or whenever a WRITE or FORMAT command is written into the WD1014. It is reset by COVF = 1 (SBEF) if L = 0, or until an additional 4 bytes have been accepted by the EDS if L = 1.

INTERRUPT REQUEST

Two latches are provided to handle interrupts. The programmed I/O interrupt (PINT) latch is set whenever an interrupt is desired at the start of data transmission to the host. The DMA interrupt (DINT) latch is set whenever an interrupt is desired at the end of data transmission to the host.

Both latches are reset when:

1. A $\overline{MR}$ occurs
2. Any command is transmitted
3. The output signal $\overline{HCS}$ is activated.

As in the case of DRQ, the true condition of INTRQ can only be sampled by external circuitry if WAUP = 0.

MISCELLANEOUS CONTROL SIGNALS

The rest of the output signals are purely combinatorial in nature and are best described by Boolean expressions. Refer to Section 3 for a description of these signals.

1. $\overline{HSC} = \overline{BUSY} \cdot \overline{CSO} \cdot A2 \cdot A1 \cdot A0 \cdot \overline{RE}$
2. $\overline{HBC} = \overline{BUSY} \cdot \overline{CSO} \cdot HSC$
3. $\overline{LUB} = \overline{CS1} \cdot \overline{A2} \cdot A1 \cdot A0 \cdot \overline{WE}$
4. $\overline{LLB} = \overline{CS1} \cdot \overline{A2} \cdot A1 \cdot \overline{A0} \cdot \overline{WE}$
5. $\overline{RCS} = \overline{COVF}\,(\overline{CSO} \cdot \overline{A2} \cdot \overline{A1} \cdot \overline{A0} + \overline{BCS})$
6. $\overline{HDCS} = (\overline{BUSY} \cdot A2 \cdot A1 \cdot A0 \cdot + \overline{BUSY} \cdot \overline{A2} \cdot \overline{A1} \cdot \overline{RE} + \overline{CSO}) -$

In words, $\overline{HDCS}$ is active only if the host is not accessing the error, status or the command registers of the WD1010 device, and $\overline{CSO}$ is aserted.

7. $\overline{CINC} = \overline{COVF} \cdot \overline{RSC}\,(\overline{WE} + \overline{RE})$
8. CMR = $\overline{MR}$ + CST where CST = $\overline{BUSY}.\overline{CSO}.A2.A1.A0.\overline{WE}$ (Any cmd written)
9. SBEF = COVF

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias ..... 0°C to 50°C
Voltage on any pin
with respect to V_{SS} ..... −0.2V to +7.0V
Power dissipation ..... 1.5 Watt

STORAGE TEMPERATURE

Plastic ..... −55°C to +125°C
Ceramic ..... −55°C to +150°C

NOTE 4:
Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

TIMING DIAGRAMS

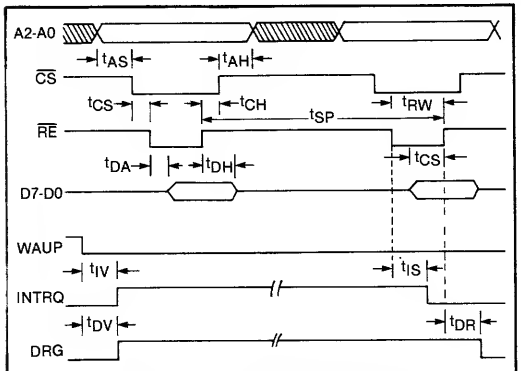


Figure 1. DATA READ CYCLE

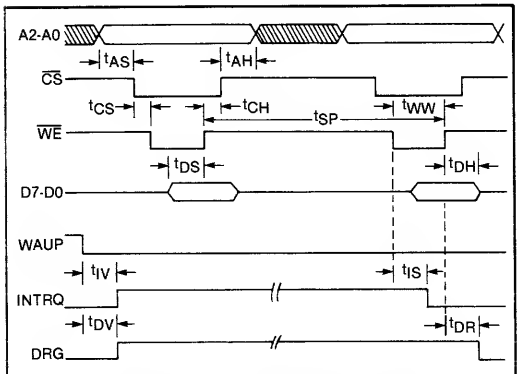


Figure 2. DATA WRITE CYCLE

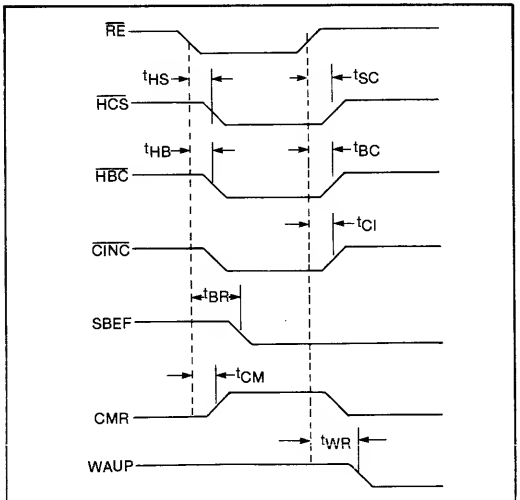


Figure 3. OUTPUT SIGNALS W.R.T. RE

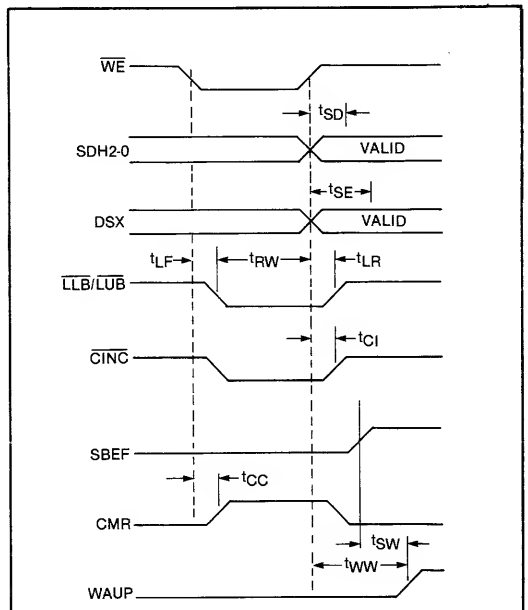


Figure 4. OUTPUT SIGNALS W.R.T. WE

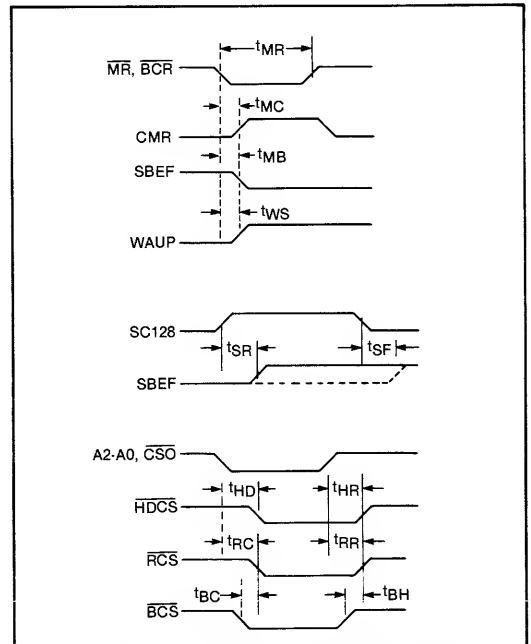


Figure 5. MISCELLANEOUS TIMINGS

See page 481 for ordering information.

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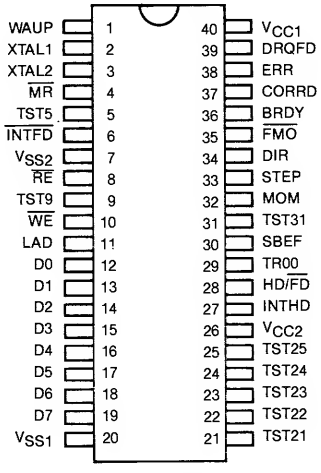
ADVANCED INFORMATION

WD1015 Buffer Manager Control Processor

FEATURES

- SINGLE +5V POWER SUPPLY
- COMPLETE BUFFER MANAGER
- PROGRAMMABLE SECTOR SIZES — 128, 256, 512, OR 1024 BYTES
- ECC BURST ERROR CORRECTION UP TO 5 BITS ON HARD DISK DATA
- 8 BIT MULTIPLEXED ADDRESS/DATA I/O BUS
- FLOPPY DISK COMMAND TRANSLATION
- SUPPORTS MOTOR ON OR HEAD LOAD DRIVES
- SUPPORTS 250 OR 500 KBS FLOPPIES
- BUFFERED SEEKS WITH FLOPPIES AND WINCHESTERS
- 16 POPULAR STEPPING RATES AVAILABLE
- AUTOMATIC RETRIES ON ALL ERRORS WITH SIMULATED COMPLETION
- POWER-ON DIAGNOSTICS INCLUDED
- 10 MHZ CLOCK RATE
- 40 PIN DIP PACKAGE



PIN DESIGNATION

DESCRIPTION

The WD1015 is a complete Control Processor (CP) that is used to handle all aspects of buffer management, in conjunction with the EDS (WD1014) device, for the Winchester/Floppy Controller board (WD1002-05). It executes all of the commands used by the WD1002-05 and does all of the control required except for real time processing, which is done by the WD1014. Throughout this specification this device will be referred to as the WD1015, or BMAC (buffer manager and controller), or simply as the CP (control processor). The WD1015 is programmed to control the transfer of information within the WFC and it maintains the necessary copies of the task files (TSF) found on both drives. Host access to the WFC causes the CP to access task file information in the TSF after a command is issued. Depending on the command, the CP will make the buffer accessible to the host or the WD1010 or 2797 controllers. The CP also controls the operation of the Error Correcting logic. During the transfer of data from the host to the WD1010, the EDS monitors the data bus, if so enabled, to compute a 4 byte ECC which is appended to the end of data transferred to the WD1010 and recorded on the disk. During data transfers from the WD1010 to the host the CP uses the ECC to validate the data. If data is corrupted the CP envokes recovery techniques such as retries and correction. A maximum of 8 retries are attempted if two consecutive syndromes do not match. Correction is attempted only if two consecutive syndromes match. If the error is uncorrectable, the operation is terminated. The CP is also used to handle data transfers from/to the SF for the floppy disk controller, which only uses CRC check bytes for its data fields. Two commands, RESTORE and SEEK, are directly executed by the CP rather than the WD2797 floppy disk controller. During status reads by the host, the CP consolidates the normal completion status from the WD1010, the WD2797 and the current EDS status into a form consistant with established WD1010 error reporting. This consolidated status is then presented to the host. The WD1015 is fabricated using HMOS technology and is available in a 40 pin DIP package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	WAKE-UP	WAUP	This input is used by the BMAC to poll a command from the host. The BUSY status bit is set immediately except in case of a WRITE/ FORMAT command. In that case, WAUP and BUSY, are set only after the sector buffer has been filled by the host. WAUP is reset when the command has been executed.
2	CRYSTAL 1	XTAL1	One side of crystal input for internal oscillator. Also input for external source.
3	CRYSTAL 2	XTAL2	Other side of crystal/external source input. Frequency should be 10 MHz.
4	MASTER RESET	$\overline{MR}$	This input is used to initialize the internal logic of the processor.
5	TEST 5	TST5	This input is to be left open by the user. Internal pullup — 300K ohm.
6	FLOPPY DISK INTERRUPT	$\overline{INTFD}$	Initiates an interrupt if interrupt is enabled; disabled on reset.
7	V_{SS2}	V_{SS2}	This input is to be left open by the user. Internal pullup — 10M ohm.
8	READ ENABLE	$\overline{RE}$	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
9	TEST 9	$\overline{TST9}$	This output is left open by the user.
10	WRITE	$\overline{WE}$	Output strobe during a BUS write. Used as write strobe to an external device. Signifies that valid data has been put on the BUS.
11	ADDRESS LATCH	LAD	This output signal occurs once during each instruction cycle. The negative edge of LAD strobes address into an external latch, used to communicate to the WD1010, WD2797, and the WD1014 chips.
12-19	DATA BUS	D7-D0	True I/O bidirectional BUS which can be written to or read synchronously using $\overline{RE}$, $\overline{WE}$, strobes. Also contains the address and data during an external acess to/from port devices, under control of LAD, $\overline{RE}$, and $\overline{WE}$.
20	GROUND	V_{SS1}	Ground.
21-25	TEST 21-25	TST21-25	Unused pins to be left open by the user.
26	V_{CC2}	V_{CC2}	+5V during operation.
27	HARD DISK INTERRUPT	INTHD	This input is polled to sense an interrupt from the WD1010, indicating completion of command issued to it by the BMAC.
28	HARD DISK/FLOPPY DISK	HD/$\overline{FD}$	This input is used to sense hard disk operation when high, and floppy disk operation when low.
29	TRACK 00	TR00	This input indicates that the R/$\overline{W}$ heads of the selected floppy drive are positioned over the outermost cylinder.
30	SECTOR BUFFER EMPTY/FULL	SBEF	This input to the BMAC is set high whenever a sector of data has been written to or read from the sector buffer.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	TEST 31	TST31	Normally left open by the user.
32	MOTOR MODE	MOM	Input used to select motor-on or head load timings for floppies. This line should be left open for motor-on type drives such as the mini floppies. A delay of 1 second will be observed before $\overline{FMO}$ is activated. For head load type drives like the standard floppies, this input should be grounded. A delay of 40 mS, will be observed before $\overline{FMO}$ is activated, thereby improving the overall performance when accessing the floppies.
33	STEP	STEP	The STEP output is pulsed once for each cylinder to be stepped on the floppies. The step pulse period is normally determined by the stepping rate selected. On a RESTORE for the floppies, however, a stepping rate of 8 mS, is used if the specified stepping rate is faster than 8 mS.
34	DIRECTION	DIR	This output is used by the floppy drive to determine the direction of a seek operation. A low defines direction as out and a high specifies direction as in.
35	FLOPPY MOTOR-ON	$\overline{FMO}$	This output is used to turn the motor on, on all floppy drives supported by the WD1002 WFC board. The drives must be configured such that the heads are loaded when this signal is activated. When the floppies are being accessed for the first time, a delay as determined by MOM, is observed before activating $\overline{FMO}$. Motor on is turned off after — 3 seconds, if no further floppy accesses are made.
36	BUFFER READY	BRDY	This output signal indicates the sector buffer is ready to be accessed by an external device such as the WD1010.
37	CORRECTED DATA	CORRD	This output status indicates to the host that the BMAC has successfully corrected a data error in the data buffer, at least once. To determine if more than one correction has taken place during a multisector read, each sector specified must be reread by the host on an individual basis.
38	ERROR	ERR	Output status bit indicates that the BMAC encountered an error during the execution of a command. The error reg, on the WFC board must be read by the host to determine the type of error that occurred.
39	DATA REQUEST	DRQFD	This input indicates to the BMAC that the WD2797 has a byte of data available to be read from the disk, or requires a byte of data to be written to the floppy disk.
40	V_{CC1}	V_{CC1}	Main power supply. +5V +/−5%

See page 481 for ordering information.

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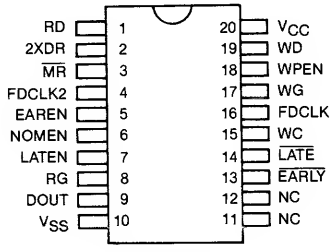
WESTERN DIGITAL
CORPORATION

WD1100-10
Write Precomp/Data Separator Support Chip

FEATURES

- COMPATIBLE WITH THE WD1010 WINCHESTER DISK CONTROLLER
- 1MHZ AND 2MHZ CLOCK OUTPUT FOR OPTIONAL FLOPPY DISK CONTROL
- EARLY/LATE/NOMINAL SIGNALS TO WRITE PRE-COMPENSATION CIRCUITRY
- SINGLE +5VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1100-10 Write Precomp/Data Separator Support Logic, when used with the WD1010 and other chips in the WD1100 series, greatly reduces the external discrete logic required to design a Winchester Hard Disk Write Precomp/Data Separator.

The WD1100-10 is fabricated in NMOS Silicon Gate Technology and is available in a 20 pin plastic or ceramic package.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
1	RD	READ DATA	This AH input is combined data and clock pulses from disk drive. (MFM)
2	2XDR	2 TIMES DATA RATE	This AH input is a 2 TIMES DATA RATE SIGNAL used to generate WC, FDCLK1 and FDCLK2.
3	$\overline{MR}$	$\overline{MASTER\ RESET}$	MR resets the clock generator.
4	FDCLK2	FLOPPY DISK CLOCK 2	This output supplies a nominal 2 MHz clock for a floppy disc controller.
5	EAREN	EARLY ENABLE	This AH output signifies the write data should be shifted early before writing.
6	NOMEN	NOMINAL ENABLE	This AH output signifies the write data should be shifted nominal before writing.
7	LATEN	LATE ENABLE	This AH output signifies the write data should be shifted late before writing.
8	RG	READ GATE	This AH input from the WD1010 or other source signifies that data is to be read from the disk.
9	DOUT	DATA OUT	This AH output data line may be 2XDR, RD, or WD depending upon the states of RG and WG.
10	V_{SS}	GROUND	Ground.
11	NC	NC	
12	NC	NC	
13	$\overline{EARLY}$	$\overline{EARLY}$	This AL input is used with $\overline{LATE}$ to derive NOMEN, EAREN and LATEN.
14	$\overline{LATE}$	$\overline{LATE}$	This AL input is used with $\overline{EARLY}$ to derive NOMEN, EAREN and LATEN.
15	WC	WRITE CLOCK	This output runs at the data rate and is 1/2 2XDR Nominal 5.0 MHz.
16	FDCLK1	FLOPPY DISK CLOCK 1	This output supplies a nominal 1 MHz clock for a floppy disk controller.
17	WG	WRITE GATE	This AH input goes high when data is to be written to the disk. Normally comes from the WD1010.
18	WPEN	WRITE PRECOMP ENABLE	This AH input enables EAREN and LATEN to be active during a write operation.
19	WD	WRITE DATA	This AH input is the WRITE DATA signal which can be gated onto DOUT.
20	V_{CC}	V_{CC}	+5 V ± 10% power supply input.

AH = ACTIVE HIGH
AL = ACTIVE LOW

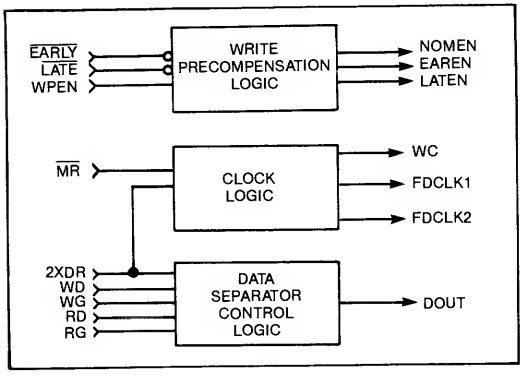


Figure 1.
WD1100-10 BLOCK DIAGRAM

DEVICE DESCRIPTION

The WD1100-10 is divided into four sections, each section will be described separately.

WRITE PRECOMPENSATION LOGIC

The $\overline{EARLY}$, $\overline{LATE}$ and WPEN input signal from the WD1010 are decoded and latched to form NOMEN, EAREN and LATEN. These three output signals are used by external circuitry to delay the write data.

CLOCK GENERATION LOGIC

The 2XDR input signal is divided to produce the output signals WC (5 MHz), FDCLK1 and FDCLK2. Both signals are symmetrical and suitable for driving WD1010 and WD279X controllers. WC is a simple divider by-two of 2XDR. FDCLK2 is derived from a symmetrical divide-by-five counter chain driven by 2XDR and FDCLK1 is derived from FDCLK2.

DATA SEPARATOR CONTROL LOGIC

The Data Separator Control Logic provides three separate operational modes by selecting one of three input sources.

IDLE MODE RG = 0, WG = 0

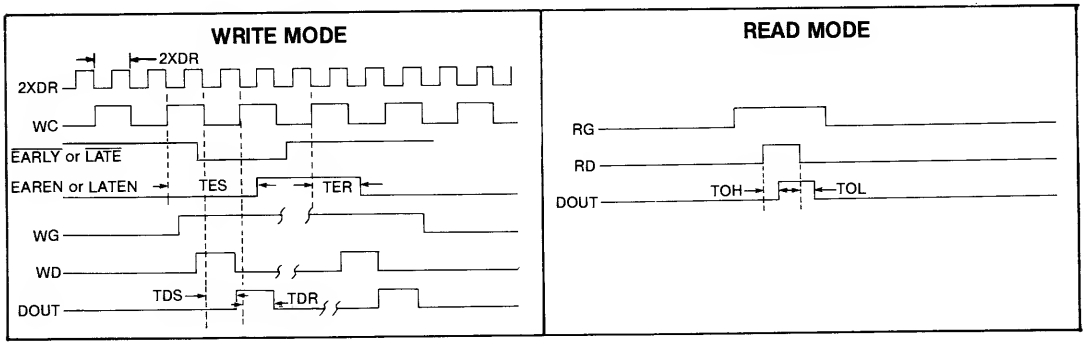
In this mode, the VCO is held locked to 2XDR. This prevents the VCO from drifting far off of the data rate when RD is not being read.

READ DATA MODE RG = 1, WG = 0

In this mode, the VCO is locked to actual data from the disk. RD is locked to the falling edge of $\overline{OSC}$. Dividing $\overline{OSC}$ with an external F/F produces RCLK. RD and RCLK are of the proper relationship to be read by the WD1010.

WRITE DATA MODE RG = X, WG = 1

In this mode, the dealy line is used to provide Write Precomp delays and at the same time the VCO is locked to WD. This accomplishes essentially the same result as locking the VCO to $\overline{2XDR}$ in the idle mode.



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COND
TES	2XDR ↓ TO EAREN ↑			2NDR + 150	NS	$\overline{EARLY}$ = 0
TER	2XDR ↓ TO EAREN ↑			2XDR + 150	NS	$\overline{EARLY}$ = 1
TDS	2XDR ↓ TO DOUT ↑			165	NS	WD = 1 WG = 1
TDR	2XDR ↓ TO DOUT ↑			165	NS	WD = 0 WG = 1
TOH	RD ↑ TO DOUT ↑			70	NS	RG = 1
TOL	RD ↓ TO DOUT ↓			70	NS	RG = 1

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... 0°C to 50°C
Voltage on any pin with
respect to V_{SS} ..... −0.2 V to +7.0 V
Power Dissipation ..... 1 Watt
Storage Temperature
Plastic ..... −55°C to +125°C
Ceramic ..... −55°C to +150°C

DC Electrical Characteristics TA = 0°C to 50°C; V_{CC} = +5 V +10% V_{SS} = 0 V

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	IOL = 3.2mA
V_{OH}	Output High Voltage	2.4			V	IOH = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

See page 481 for ordering information.

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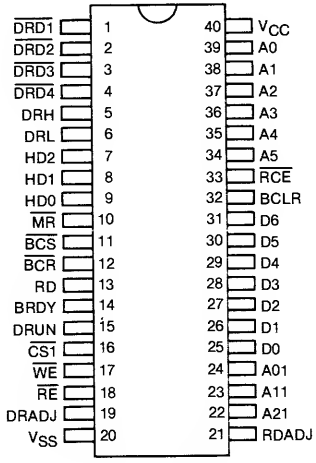
ADVANCED INFORMATION

WD1100-11 Buffer Manager Support Chip

FEATURES

- DRUN PULSE GENERATION
- RD PULSE GENERATION
- BUFFER MEMORY CONTROL
- HEAD SELECT GENERATION
- DRIVE SELECT GENERATION
- 40 PIN DUAL-IN-LINE PACKAGE
- SINGLE +5VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1100-11 Buffer Manager Support Chip controls the operation of the external buffer memory when used with the WD1010 Winchester Disk Controller. The WD1100-11 provides a means for programming the Head Select and Drive Select by latching onto the SDH information when it is available on the Data Bus. The WD1100-11 also converts the serial data from the selected drive and shapes the Read Data and DRUN pulses appropriately for the WD1010.

The WD1100-11 is designed using NMOS technology and is manufactured in a 40 pin DIP package. The WD1100-11 requires only a single +5VDC supply.

PIN DESCRIPTION

PIN NUMBER	SIGNAL	SIGNAL NAME	DESCRIPTION
1 2 3 4	$\overline{DRD1}$ $\overline{DRD2}$ $\overline{DRD3}$ $\overline{DRD4}$	$\overline{DRIVE\ DATA\ BITS\ 1\text{-}4}$	Serial data from four drives.
5 6	DRH DRL	DRIVE SELECT BITS	Selects drives 1-4 depending upon bit configuration.
7 8 9	HD2 HD1 HD0	HEAD SELECT BITS 0-2	Selects heads 1-8 depending upon bit configuration.
10	$\overline{MR}$	$\overline{MASTER\ RESET}$	Master reset.
11	$\overline{BCS}$	$\overline{BUFFER\ CHIP\ SELECT}$	WD1010 to RAM chip select.
12	$\overline{BCR}$	$\overline{BUFFER\ COUNTER\ RESET}$	Resets the external buffer counter.
13	RD	READ DATA	Strobe for reading data from the disk.
14	BRDY	BUFFER READY	This line indicates the RAM buffer is ready to read or write data.
15	DRUN	DRUN	This line informs the WD1010 when a field of 0's or 1's have been detected.
16	$\overline{CS1}$	$\overline{CHIP\ SELECT\ 1}$	Host to WD1100-11 chip select.
17	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	Write Enable strobe latches SDH value on bus and increments Sector Buffer Address Counter for write operations.
18	$\overline{RE}$	$\overline{READ\ ENABLE}$	Read Enable strobe increments Sector Buffer Address Counter for read operations.
19	DRADJ	DRUN ADJUST	DRUN pulse adjustment.
20	V_{SS}	GROUND	
21	RDADJ	RD ADJUST	RD pulse adjustment.
22 23 24	A21 A11 A01	HEAD/DRIVE SDH REGISTER SELECT BITS A21, A11, A01	These bits select the SDH register in the WD1100-11 for head and drive select programming and also select the data register during R/W sector commands.
25 26 27 28 29 30 31	D0 D1 D2 D3 D4 D5 D6	DATA BIT 0-6 ACCESS LINES	7-bit data access lines.
32	BCLR	BUFFER CLEAR	This line clears the RAM buffer.
33	$\overline{RCE}$	$\overline{RAM\ CHIP\ ENABLE}$	WD1100-11 to RAM chip enable.
34 35 36 37 38 39	A5 A4 A3 A2 A1 A0	RAM ADDRESS LINES 0-5	Address lines for accessing the external RAM buffer.
40	V_{CC}	+5VDC	

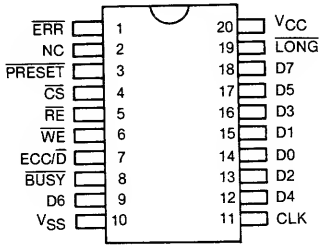
See page 481 for ordering information.

ADVANCED INFORMATION

WD1100-13 ECC Logic Device

FEATURES

- 32 BIT COMPUTER SELECTED POLYNOMIAL
- MAXIMUM BURST DETECTION SPAN-11 BITS
- PARALLEL INPUT/OUTPUT
- DATA TRANSFER RATES UP TO 5 MBITS/SEC
- RECORD LENGTH UP TO 1038 BYTES INCLUDING CHECK BYTES
- TTL, MOS COMPATIBLE
- 20 PIN, NMOS TECHNOLOGY DIP PACKAGE
- SINGLE +5VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1100-13 is designed to provide ECC capabilities for Winchester Disk Controllers and will accommodate data transfer rates of up to 5 Mbits/sec. Data is transferred into and out of the WD1100-13 via an 8 bit bidirectional parallel data port.

The WD1100-13 performs several operations including, check byte generation, error detection, and error syndrome generation. Additionally, the WD1100-13 supports user diagnostics by allowing transparent check byte transfers between the host and disk medium.

The WD1100-13 uses NMOS technology and is provided in a 20 pin DIP package configuration. Only a single +5VDC supply is required.

PIN DESCRIPTION

PIN NUMBER	SIGNAL	SIGNAL NAME	I/O	SIGNAL DESCRIPTION
1	ERR	ERROR	O	When this line is low, it indicates that no error was detected in the syndrome bytes.
2	NC	NC		NO CONNECTION
3	$\overline{\text{PRESET}}$	$\overline{\text{PRESET}}$	I	This line, when low, presents the ECC accumulator to logic ones.
4	$\overline{\text{CS}}$	$\overline{\text{CHIP SELECT}}$	I	A low input on this line enables WE and RE.
5	$\overline{\text{RE}}$	$\overline{\text{READ ENABLE}}$	I	Used to write data bytes into the ECC accumulator and read data bytes from the ECC accumulator.
6	$\overline{\text{WE}}$	$\overline{\text{WRITE ENABLE}}$	I	Used to write data bytes and check bytes into the ECC accumulator.
7	ECC/$\overline{\text{D}}$	ECC/$\overline{\text{DATA}}$	I	A logic 0 indicates that user data is being strobed for check byte computation and a logic one indicates a check/syndrome byte is being strobed.
8	$\overline{\text{BUSY}}$	$\overline{\text{BUSY}}$	O	The BUSY bit is set when the WD1100-13 is performing an input or output data transfer, thus inhibiting user access.
10	V_{SS}	GND		Ground.
9	D6	DATA BITS 0-7	I/O	8 bit parallel bidirectional bus used to transfer data bytes, check bytes, and syndrome bytes.
12	D4			
13	D2			
14	D0			
15	D1			
16	D3			
17	D5			
18	D7			
11	CLK	CLOCK	I	5 MHz clock used for internal timing within the WD1100-13.
19	$\overline{\text{LONG}}$	$\overline{\text{LONG}}$	I	When this signal is a logic one, normal mode is selected. When this signal is low, long mode is selected and PRESET is inhibited.
20	V_{CC}	+5VDC		+5VDC +10%

See page 481 for ordering information.

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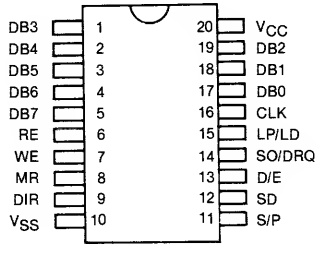
ADVANCED INFORMATION

WD1100-14 Programmable Polynomial Generator (PPG)

FEATURES

- PERFORMS THE FUNCTION OF AN 8 BYTE BY 8 BIT (64 BITS) PROGRAMMABLE POLYNOMIAL (ERROR CORRECTION CODE) GENERATOR.
- ALL BIT POSITIONS CAN BE PROGRAMMED TO PERFORM THE FUNCTION OF ERROR CORRECTION CODE CALCULATION.
- LAST BIT IS ALWAYS SET FOR CALCULATION.
- BYTE LENGTH OF THE POLYNOMIAL IS PROGRAMMABLE FROM 1 TO 8.
- DESIRED POLYNOMIAL CAN BE ENTERED IN PARALLEL OR SERIAL.
- DATA CAN BE WRITTEN TO DEVICE IN PARALLEL OR SERIAL FORM.
- ECC'S OUTPUT IS IN PARALLEL OR SERIAL FORMAT.
- WHEN GOING FROM FUNCTION OF READING ECC TO INPUT OF DATA FOR CALCULATION, DATA REGISTER IS SET TO ALL 1'S.
- WHEN A PARALLEL OPERATION IS IN PROGRESS, DRQ & LOST DATA STATUS ARE ACTIVE.
- ANY DATA TRANSFER TO AND FROM DEVICE IS TRUE DATA.
- PARALLEL I/O BUS & SERIAL I/O PIN.
- ALL LOGIC IS IMPLEMENTED WITH STATIC CIRCUITS.
- ALL INPUTS AND OUTPUTS ARE TTL COMPATIBLE.
- PACKAGED IN A 20 PIN DUAL INLINE PACKAGE.
- SINGLE 5V SUPPLY.



PIN DESIGNATION

DESCRIPTION

The WD1100-14 Programmable Polynomial Generator (PPG) is an NMOS logic device designed to be programmed for 8 bit to 64 bit polynomial byte length in 8 bit steps. The WD is designed primarily for generating ECC/CRC polynomials for Winchester control. The WD1100-14 permits greater ECC/CRC range in the transfer of data to and from Winchester disks.

The WD1100-14 requires only a single + 5VDC power source and is available in a 20-pin, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
5-1, 19-17	DATA BUS	DB7-0	I/O	I/O bus line, true, DB7 = MSB.
6	READ ENABLE	$\overline{RE}$	I	When low the contents of the 8 bit output register appear on the Data Bus. Resets DRQ pin.
7	WRITE ENABLE	$\overline{WE}$	I	When low loads the input register with the contents of the Data Bus. When a $\overline{MR}$ pulse has occurred with S/P = 0 the next 8 $\overline{WE}$'s load the 8 bytes of the polynomial register from the Data Bus. Resets DRQ pin.
8	MASTER RESET	$\overline{MR}$	I	Resets the SET latch, picks parallel or serial load of polynomial from S/$\overline{P}$ pin, and sets polynomial length latch from DIR pin.
9	DIRECTION	DIR	I	After a $\overline{MR}$ pulse : DIR = 0 selects polynomial length of 8 bytes, DIR = 1 selects a programmable polynomial length. This is 1 of 3 control pins for the functions of the chip.
10	GROUND	V_{SS}	P	Device ground.
11	SERIAL/PARALLEL	S/$\overline{P}$	I	After a $\overline{MR}$ pulse : S/$\overline{P}$ = 0 selects 8 byte parallel load of polynomial register, S/$\overline{P}$ = 1 selects serial load of polynomial register through DB7. This is 1 of 3 control pins for the functions of the chip.
12	SERIAL DATA	SD	I/O	Tri-state I/O pin for serial data to and from the chip, controlled by DIR, S/$\overline{P}$, and D/$\overline{E}$.
13	DATA/ECC	D/$\overline{E}$	I	For D/$\overline{E}$ = 0 to 1 transition a set sequence is initiated to set the data register to all 1's. On any transition resets DRQ and LD pins. This is 1 of 3 control pins for the functions of the chip.
14	SERIAL OUTPUT/ DATA REQUEST	SO/DRQ	O	When S/$\overline{P}$ = 1 this is a Serial Output from the data register. When S/$\overline{P}$ = 0 this the Data Request Output.
15	LOAD POLYNOMIAL/ LOST DATA	LP/LD	I/O	When S/$\overline{P}$ = 1 this is an input pin that when pulsed high Loads the Polynomial register with the contents of the data register. When S/$\overline{P}$ = 0 this is the Lost Data output.
16	CLOCK	CLK	I	Master clock for device.
20	V_{CC}	V_{CC}	P	+ 5V power supply.

See page 481 for ordering information.

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PRELIMINARY

WD1000-05 Winchester Disk Controller

FEATURES

- BUILT IN DATA SEPARATOR
- BUILT IN WRITE PRECOMPENSATION LOGIC
- CONTROL FOR UP TO 4 WINCHESTER DRIVES
- CONTROL FOR UP TO 8 READ/WRITE HEADS
- 1024 CYLINDER ADDRESSING RANGE
- 256 SECTOR ADDRESSING RANGE
- CRC GENERATION/VERIFICATION ON ID FIELDS
- AUTOMATIC FORMATTING
- 128, 256, 512, 1024 USER SELECTABLE BYTES PER SECTOR
- UNLIMITED SECTOR INTERLEAVE CAPABILITY
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS
- MFM ENCODING RECORDING
- AUTOMATIC RETRIES ON ALL ERRORS
- PROGRAMMABLE 500 μSEC INCREMENTAL STEP PULSE RATES (35 μS TO 7.5 mS)
- AUTOMATIC RESTORE ON ALL SEEK ERRORS
- PROGRAMMABLE DISK PARAMETERS
- ERROR REPORTING (DISK/CONTROLLER)
- 8 BIT HOST INTERFACE
- SINGLE +5VDC SUPPLY

DESCRIPTION

The WD1000-05 Winchester Disk Controller is a stand alone, general purpose Winchester disk drive controller board designed to interface up to four Winchester disk drives with a host processor. The drive signals are based upon the Floppy look-alike interface available on the Seagate Technology ST506, the Quantum Q2000, and other compatible drives.

Communications to and from the host processor are made via a separate computer access port. This port consists primarily of an 8-bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro commands are transferred via this 8 bit bus. An on-board sector buffer allows data transfers to the host computer independant of the actual drive data transfer rate.

The WD1000-05 is based upon a proprietary chip set consisting of the WD1010, the WD1100-11, and the WD1100-10 designed specifically for Winchester drive control.

ARCHITECTURE

The WD1000-05 has seven on board connectors. These connectors consist of a power connector, host interface connector, drive control connector, and four high speed data cable connectors. The drive control cable is daisy-chained to each of the four drives.

The drive data connectors carry differential signals and are radially connected. Up to four drives can be accommodated by the WD1000-05.

The host interface connector provides interface signals that are compatible with most microprocessors and mini-computers.

SPECIFICATIONS

Encoding method:	MFM
Cylinders per Head:	Up to 1024
Sectors per Track:	Up to 256 (1024 byte sec)
Heads:	8
Drive Selects:	4
Step rate:	7.5 mS to 35 μS (0.5 mS increments)
Data Transfer Rate:	5 Mbits/sec
Write Precomp Time:	12 Nanoseconds
Sectoring:	Soft
Host Interface:	8 Bit bi-directional bus
Drive Capability:	10 "LS" Loads
Drive Cable Length:	10 ft. (3M) max.
Host Cable Length:	3 ft. (1 M) max.
Power Requirements:	+5V ±5%, 3.0A Max. (2.5A typ.)
Ambient Temperature Operating:	0°C to 50°C (32 F to 122 F)
Relative Humidity:	20% to 80%
MTBF:	10,000 POH
MTTR:	30 minutes

DIMENSIONS

Length:	8 in. (20.3 cm)
Width:	5.75 in. (14.5 cm)
Height:	0.75 in. (1.9 cm)

HOST INTERFACING

The WD1000-05 is designed to easily interface to most micro computers and mini-computers. All interfacing is done through the Host Interface Connector (J5). The interface is very similar to Western Digital's family of Floppy Disk Controllers.

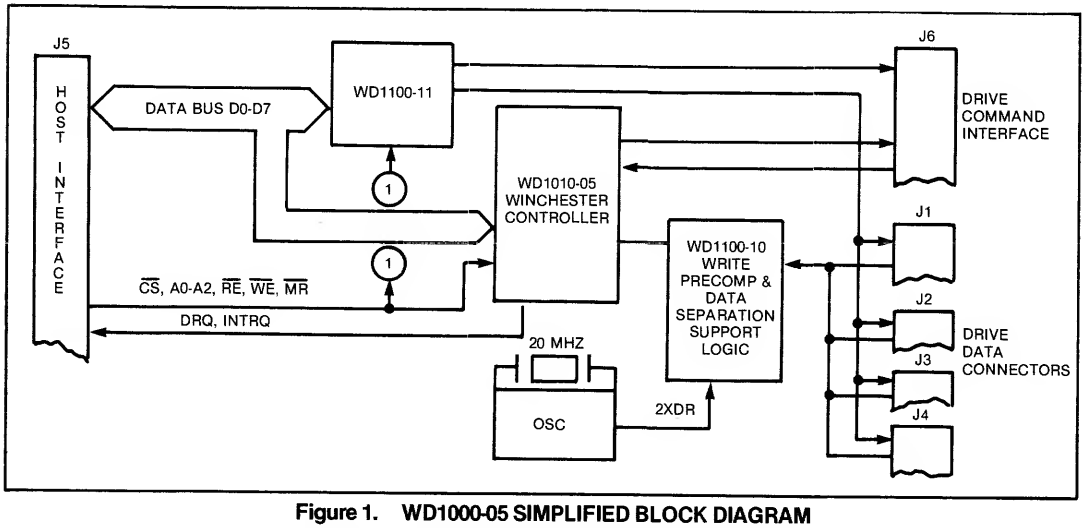


Figure 1. WD1000-05 SIMPLIFIED BLOCK DIAGRAM

Table 1. HOST INTERFACE CONNECTOR

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the CS line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When Card Select is active along with RE or WE, Data is read or written via the DAL bus. CS must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with CS, the host may write data to a selected register of the WD1000-05.
28	27	$\overline{RE}$	When Read Enable is active along with CS, the host may read data from a selected register of the WD1000-05.
30	29	PULLED UP (PUP)	
32	31	Not Connected	
34	33	Not Connected	
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.

Table 1. HOST INTERFACE CONNECTOR (Continued)

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
38	37	DRQ	The Data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the Data Register is read from or written to. The DRQ line will continue to toggle until the buffer is exhausted or until a write or read is performed on the Cylinder Low register.
40	39	$\overline{MR}$	The Master Reset line initializes all internal logic on the logic on the WD1000-05. Sector Number, Cylinder Number and SDH are cleared, stepping rate is set to 7.5 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ and INTRQ lines are reset. The Drive Select register is set to 1.
	41-50	Not Connected	
Note: Grounds			All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J7, pins 2 & 3.

DRIVE CONTROL CONNECTORS

The drive control connector is a (relatively) low speed bus that is daisy chain connected to each of the drives (up to four) in the system. To properly terminate each TTL level output signal from the WD1000-05, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. All other drives should have no termination. See Table 2:

Table 2. 34 PIN DRIVE CONTROL CONNECTOR

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	$\overline{RWC}$
3	4	O	$\overline{Head\ Select\ 2}$
5	6	O	$\overline{Write\ Gate}$
7	8	I	$\overline{Seek\ Complete}$
9	10	I	$\overline{TR000}$
11	12	I	$\overline{Write\ Fault}$
13	14	O	$\overline{Head\ Select\ 0}$
15	16	NC	
17	18	O	$\overline{Head\ Select\ 1}$
19	20	I	$\overline{Index}$
21	22	I	$\overline{Ready}$
23	24	O	$\overline{Step}$
25	26	O	$\overline{Drive\ Select\ 1}$
27	28	O	$\overline{Drive\ Select\ 2}$
29	30	O	$\overline{Drive\ Select\ 3}$
31	32	O	$\overline{Drive\ Select\ 4}$
33	34	O	$\overline{Direction\ In}$

DRIVE CONTROL SIGNAL DESCRIPTIONS

$\overline{RWC}$

When the Reduce Write Current line is activated with Write Gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The $\overline{RWC}$ line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

$\overline{Write\ Gate}$

This output signal allows data to be written on the disk.

$\overline{Seek\ Complete}$

Informs the WD1000-05 that the head of the selected drive has reached the desired cylinder and has stabilized. Seek Complete is not checked after a SEEK command, thus allowing overlapped seeks.

$\overline{Track\ 000}$

Indicates that the R/W heads are positioned on the outer-most cylinder. This line is sampled immediately before each step is issued.

$\overline{Write\ Fault}$

Informs the WD1000-05 that some fault has occurred on the selected drive. The WD1000-05 will not execute commands when this signal is true.

$\overline{HS0\text{-}HS2}$

Head Select lines are used by the WD1000-05 to select a specific R/W head on the selected drive.

$\overline{Index}$

Is used to indicate the index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

$\overline{\text{Ready}}$

Informs the WD1000-05 that the desired drive is selected and that its motor is up to speed. The WD1000-05 will not execute commands unless this line is true.

$\overline{\text{Step}}$

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the $\overline{\text{DIRECTION IN}}$ line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the SEEK COMPLETE time from the drive.

$\overline{\text{Direction In}}$

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

$\overline{\text{DS1-DS4}}$

These four Drive Select lines are used to select one of four possible drives.

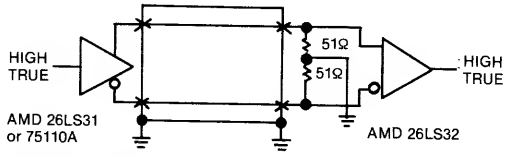
DRIVE DATA CONNECTOR

Four data connectors (J1-J4) are provided for clock signals and data between the WD1000-05 and each drive. All lines associated with the transfer of data between the drive and the WD1000-05 system are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers. The cable used should be flat ribbon cable or twisted pair with a length of less than 10 feet. The cable pin-outs are per Table 4:

Table 3. DATA CONNECTIONS AND DESCRIPTIONS

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1		NC
4	3		NC
6	5		NC
8	7		NC
	9		NC
	10		NC
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	– MFM Read Data
19			GND
20			GND

DIFFERENTIAL DATA DRIVER/RECEIVER



NOTE: ANY RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE

$Z_\chi = 105\Omega$ FLAT RIBBON OR TWISTED PAIR MAX 10 FT.

POWER CONNECTOR

A four pin connector (J7) is provided for power input to the WD1000-05. See Table 4.

Table 4.

PIN	WD1001-05
1	Not Connected
2	Ground
3	Ground
4	+5V Regulated
Housing	Amp 1-4840429-0

TASK FILE

The Task File is a bank of registers used to hold parameter information pertaining to each command. These registers and their addreses are:

A_2	A_1	A_0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE:
Registers are **not** cleared by master reset (MR).

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC	—	ID	—	AC	TK	DM

Bit 7 — Bad Block Detect
This bit is set when an ID field has been encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 — CRC Data Field
This bit is set when a data field CRC error has occurred or the Data Address Mark has not been found. The sector buffer may still be read but will contain errors.

Bit 5 — Reserved
Not used; forced to a zero.

Bit 4 — ID Not Found
This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk, or if an ID field CRC error has occurred.

Bit 3 — Reserved
Not used; forced to a zero.

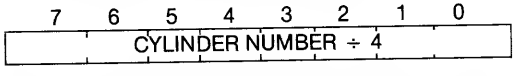
Bit 2 — Aborted Command
This bit is set if a command was issued while the DRDY (Pin 28) line is low or the WF (Pin 30) line is low. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 — TK000 Error
This bit is set only by the restore command. It indicates that the TK000 (Pin 31) line has not gone active after the issuance of 1024 stepping pulses.

Bit 0 — Data Address Mark Not Found
This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.

WRITE PRECOMP CYLINDER

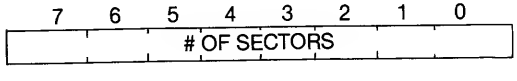
This register is used to define the cylinder number where the RWC (Pin 33) line is asserted:



The value (0-255) loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus, a value of H'01' will cause RWC to activate on cylinder 4; H'02' on cylinder 8, and so on. Switching points are then 0, 4, 8, . . . 1020. The RWC will be asserted when the present cylinder is equal to a greater than the value in this register. For example, the ST506 requires precomp on cylinder 128 (H'80') and above. Therefore, the write precomp cylinder register should be loaded with 32 (H'20').

SECTOR COUNT

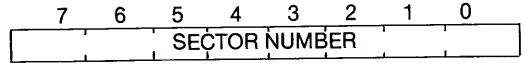
This register holds the number of sectors that are needed to be transferred to the buffer:



This register is used during a multiple sector R/W command. The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

This register holds the sector number of a desired sector:



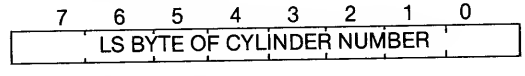
During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from 0 to 255.

CYLINDER REGISTERS

Internal to the WD1000-05, is another pair of registers that hold the actual position number where the R/W heads are located. The cylinder number high and low registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WD1000-05 automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a Restore.

CYLINDER NUMBER LOW

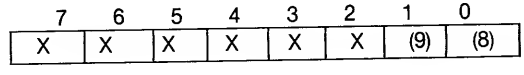
This register holds the least significant 8 bits of the desired cylinder number:



It is used in conjunction with the cylinder number high register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH

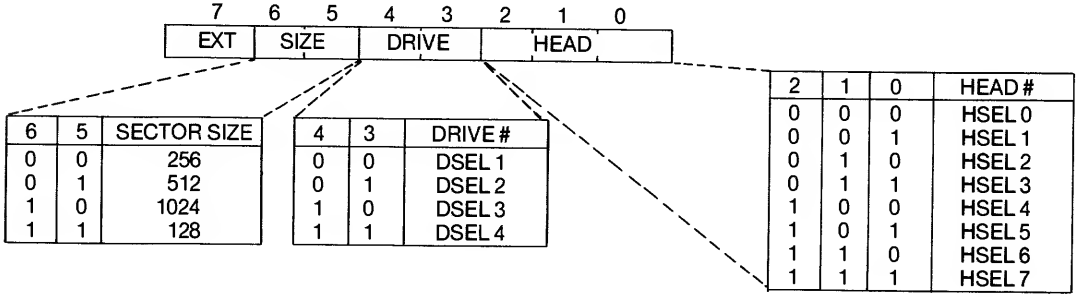
This register defines the two most significant bits of the cylinder number desired:



SDH BYTE

This register contains the desired sector size, drive number, and head number parameters.

Bit 7, the extension bit, is used to extend the data field by seven bytes when using ECC codes. CRC is not appended to the end of the data field when EXT = 1; the data field becomes "sector size + 7" bytes long. CRC is checked on the ID field regardless of the state of the extension bit. Note that the sector size bits are written to the ID during a formatting command. The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written but does have bad block mark written. The format is:



6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the WD1010 as well as reporting status from the drive control lines. The format is:

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	—	CIP	ERR

Bit 7 — Busy
This bit is set whenever the WD1010 is accessing the disk. Commands should not be loaded into the command register while busy is set. Busy is made active when a command is written into the WD1010 and is deactivated at the end of all commands except the read sector. While executing a read sector command, busy is deactivated after the sector buffer has been filled.

Bit 6 — Ready
This pin normally reflects the state of the DRDY (Pin 28) line.

Bit 5 — Write Fault
This bit reflects the state of the WF (Pin 30) line. Whenever the WF pin goes high, an interrupt will be generated.

Bit 4 — Seek Complete
This bit reflects the state of the SC (Pin 32) line. Certain commands will pause until seek complete is true.

Bit 3 — Data Request
This bit reflects the state of the BDRQ (Pin 36) line. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command. DRQ/BDRQ remains high until BRDY is sensed, indicating the operation is completed. The BDRQ signal can be used in DMA interfacing, while the DRQ bit can be used for programmed I/O transfers.

Bit 2 — Reserved
Not used. This bit is always forced to a zero.

Bit 1 — Command in Progress
When this bit is set, a command is being executed

and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host.

Bit 0 — Error
This bit is set whenever any bits in the error register are set. It is the logical 'or' of the error register and may be used by the host to quickly check successful completion of a command. This bit is reset when a new command is written into the command register.

COMMAND REGISTER

This write-only register is loaded with desired command:

7	6	5	4	3	2	1	0
		C	O	M	M	A	N	D		

The commands begins to execute immediately upon loading. This register should not be loaded while the Busy or CIP bits are set in the status register. The INTRQ (Pin 3) line, if set, will be cleared by a write to the command register.

COMMANDS

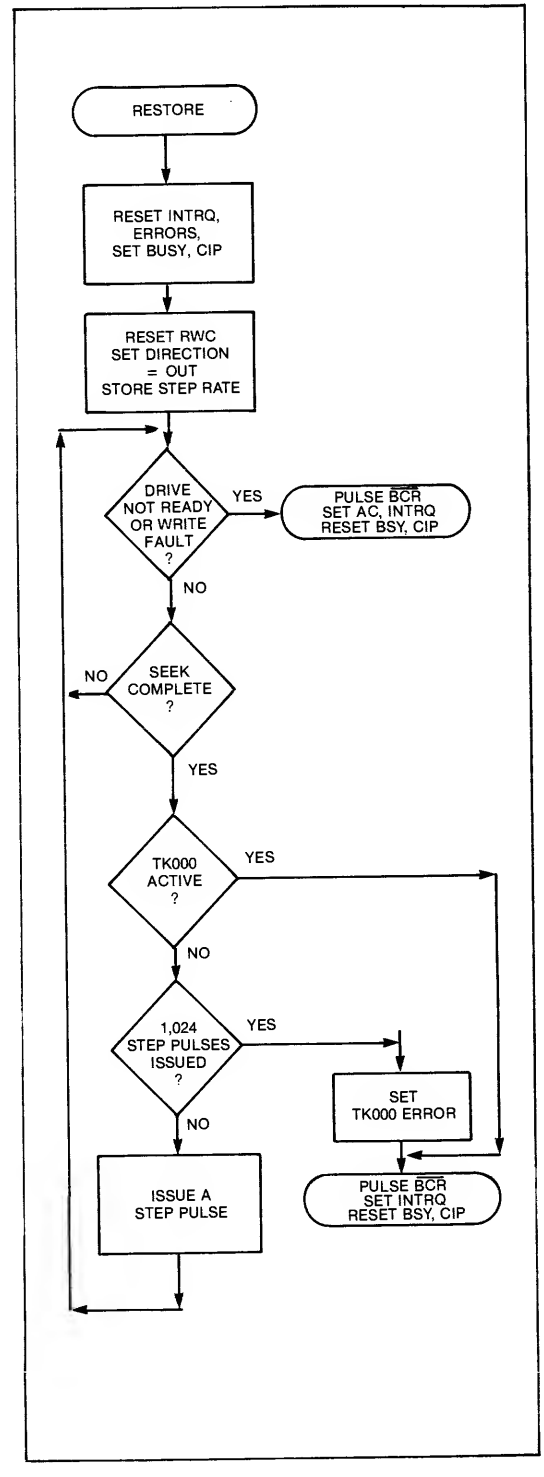
The WD1000-05 will execute six commands. Prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

COMMAND SUMMARY

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R_3	R_2	R_1	R_0
SEEK	0	1	1	1	R_3	R_2	R_1	R_0
READ SECTOR	0	0	1	0	I	M	0	0
WRITE SECTOR	0	0	1	1	0	M	0	0
SCAN ID	0	1	0	0	0	0	0	0
WRITE FORMAT	0	1	0	1	0	0	0	0

R_3-R_0 Rate Field

For 5 MHz WCLK:
R_3-R_0 = 0000 — ≈35 μs.
0001 — .5 ms.
0010 — 1.0 ms.
0011 — 1.5 ms.
0100 — 2.0 ms.
0101 — 2.5 ms.
0110 — 3.0 ms.
0111 — 3.5 ms.
1000 — 4.0 ms.
1001 — 4.5 ms.
1010 — 5.0 ms.
1011 — 5.5 ms.
1100 — 6.0 ms.
1101 — 6.5 ms.
1110 — 7.0 ms.
1111 — 7.5 ms.



Bit 0, ("T") Read Sector, Write Sector Commands

Should be set to 0 for WD1000-05

M = Multiple Sector Flag

M = 0 Transfer 1 sector
M = 1 Transfer multiple sectors

I = Interrupt Enable

I = 0, Interrupt at BDRQ time
I = 1, Interrupt at end of command

RESTORE COMMAND

The restore command is usually used on a power-up condition. The actual stepping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1000-05 waits for the Seek Complete line to go active before issuing the next pulse. If after 1,024 stepping pulses, the TK000 line does not go active, the WD1000-05 will set the TK000 error bit in the error register and terminate with an INTRQ. An interrupt will also occur if the write fault goes active or the DRDY goes inactive during execution.

The rate field specified (R_3-R_0) is stored in an internal register for future use in commands with implied seeks.

SEEK COMMAND

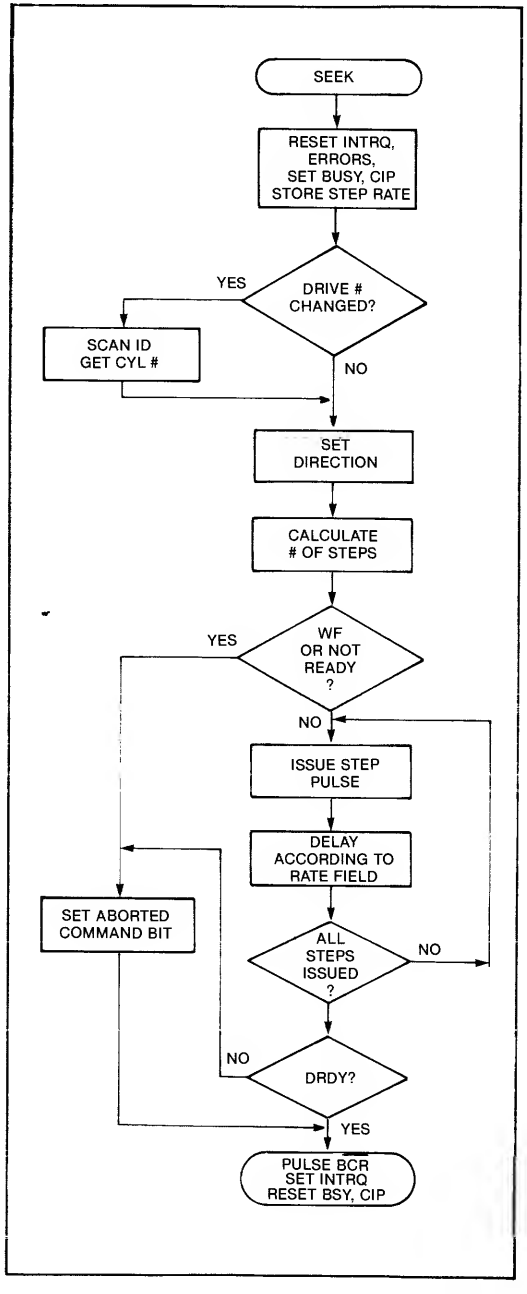
Since all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The actual step rate used is taken from the rate field, which is also stored in an internal register for future use. If DRDY goes inactive or WF goes active, the command is terminated and an INTRQ is generated.

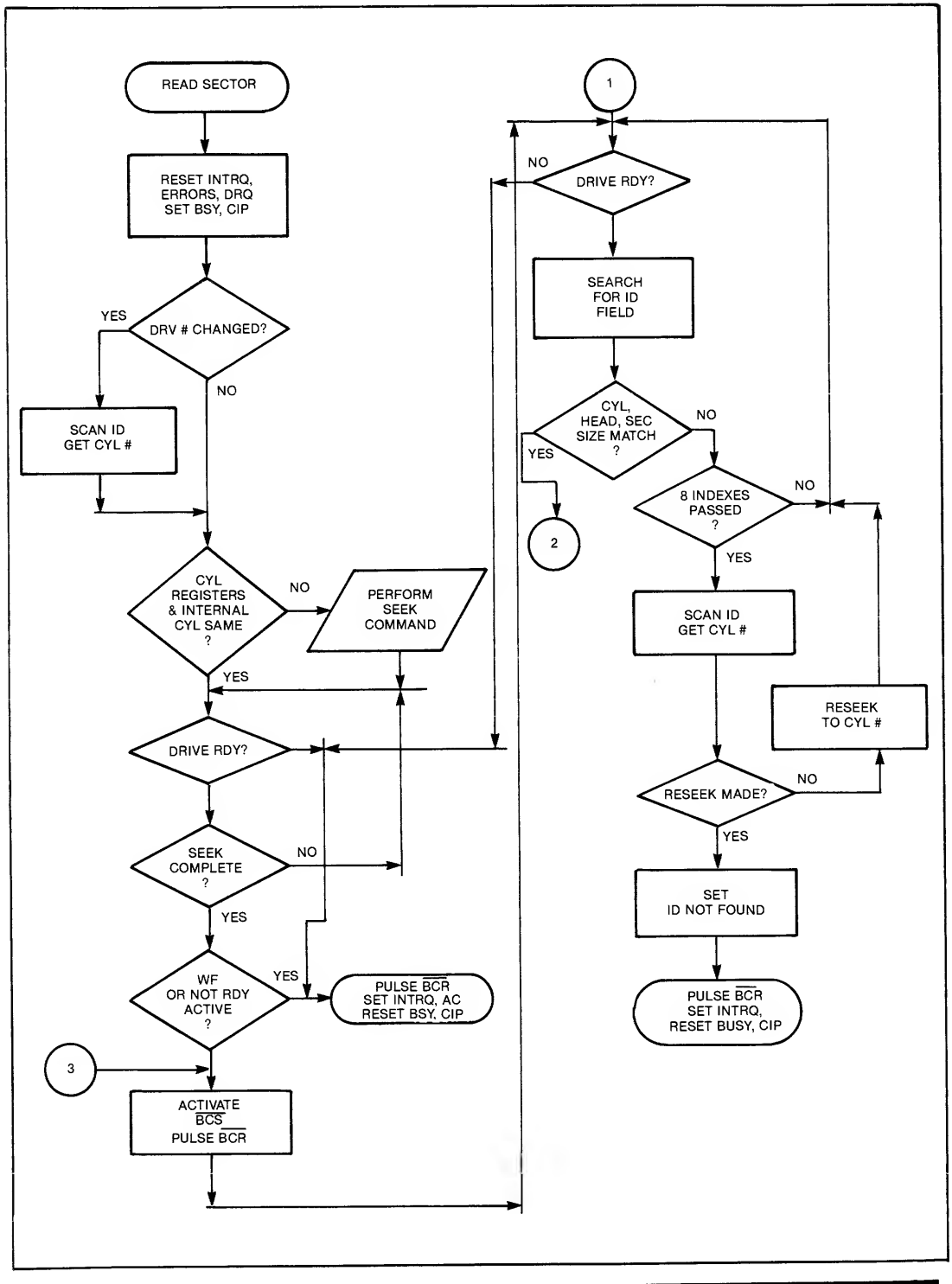
The direction and number of step pulses needed are calculated by comparing the contents of the cylinder register high/low to the cylinder position number stored internally. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. Seek complete is not checked at the beginning or end of the command.

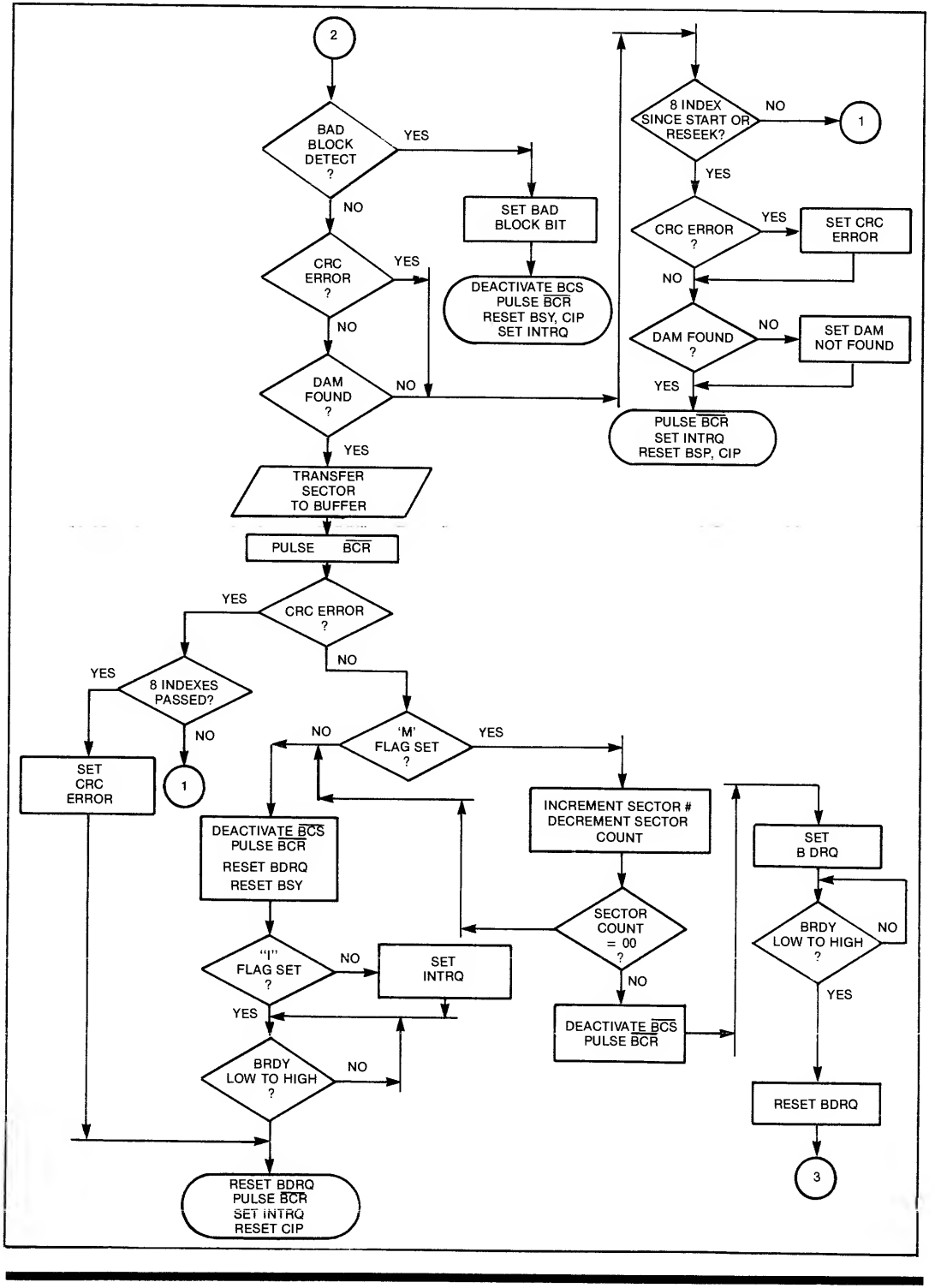
READ SECTOR

The read sector command is used to transfer one or more sectors of data to the disk. Upon receipt of this command, the WD1000-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and a seek takes place. Write Fault and DRDY lines are checked throughout the command.

After seek complete is found to be true (with or without an implied seek), the search for an ID field occurs. The WD1000-05 must find an ID with the correct cylinder, head, sector size, and CRC within 8 revolutions or else the appropriate error bits will be set and the command terminated. If not, eight retries are performed with the ID-NOT-FOUND error bit set and the command terminated. Both the Read and Write sector commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command.




READ SECTOR
RESET INTRQ, ERRORS, DRQ SET BSY, CIP
DRV # CHANGED?
YES
NO
SCAN ID GET CYL #
CYL REGISTERS & INTERNAL CYL SAME ?
NO
PERFORM SEEK COMMAND
YES
DRIVE RDY?
SEEK COMPLETE ?
NO
YES
WF OR NOT RDY ACTIVE ?
YES
PULSE BCR SET INTRQ, AC RESET BSY, CIP
3
ACTIVATE BCS PULSE BCR
1
NO
DRIVE RDY?
SEARCH FOR ID FIELD
CYL, HEAD, SEC SIZE MATCH ?
NO
YES
2
8 INDEXES PASSED ?
NO
YES
SCAN ID GET CYL #
RESEEK TO CYL #
RESEEK MADE?
NO
YES
SET ID NOT FOUND
PULSE BCR SET INTRQ, RESET BUSY, CIP


2
BAD BLOCK DETECT ?
YES
SET BAD BLOCK BIT
DEACTIVATE BCS
PULSE BCR
RESET BSY, CIP
SET INTRQ
NO
CRC ERROR ?
YES
NO
DAM FOUND ?
NO
YES
TRANSFER SECTOR TO BUFFER
PULSE BCR
YES
CRC ERROR ?
NO
YES
8 INDEXES PASSED?
NO
SET CRC ERROR
1
NO
'M' FLAG SET ?
YES
DEACTIVATE BCS
PULSE BCR
RESET BDRQ
RESET BSY
"I" FLAG SET ?
NO
SET INTRQ
YES
BRDY LOW TO HIGH ?
NO
RESET BDRQ
PULSE BCR
SET INTRQ
RESET CIP
INCREMENT SECTOR #
DECREMENT SECTOR COUNT
SECTOR COUNT = 00 ?
NO
DEACTIVATE BCS
PULSE BCR
8 INDEX SINCE START OR RESEEK?
NO
1
YES
CRC ERROR ?
YES
SET CRC ERROR
NO
DAM FOUND ?
NO
SET DAM NOT FOUND
YES
PULSE BCR
SET INTRQ
RESET BSP, CIP
SET B DRQ
BRDY LOW TO HIGH ?
NO
YES
RESET BDRQ
3

When the data address mark is found, the WD1000-05 is ready to transfer data to the buffer. After the sector data has been transferred, the I flag is checked. If the I flag is 0, the INTRQ is made active coincident with BDRQ, indicating a transfer of data is required by the host. If I = 1, the INTRQ will occur at the end of the command (i.e. after the buffer is unloaded by the host).

An optional M flag may be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1000-05 decrements the sector count register and increments the sector number register. The next logical sector will be transferred, regardless of the interleave. Sectors are numbered at format time by a byte in the ID field.

For the WD1010 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. The sector transfers will continue until the sector count register equals zero or BRDY goes inactive. If the sector count register is non-zero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the next sector in this multiple sector read command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1000-05:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 0 (On).
(3)	1000-05:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1000-05:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(5)	1000-05:	Sets BDRQ = 1; sets DRQ flag.
(6)	1000-05:	If I bit = 1 then (9).
(7)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$).
(8)	1000-05:	Waits for BDRY then sets INTRQ = 1; End.
(9)	1000-05:	Sets INTRQ = 1.
(10)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$); End.

When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1000-05:	Strobes $\overline{BCR}$; set $\overline{BCS}$ = 0 (On).
(3)	1000-05:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1000-05:	Decrements sector count register; increments sector number register.
(5)	1000-05:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(6)	1000-05:	Sets BDRQ = 1; DRQ flag = 1.
(7)	Host:	Reads out content of buffer (by $\overline{RE}$ strobes).
(8)	Buffer:	Indicates data has been transferred by asserting BRDY.
(9)	1000-05:	When BRDY is asserted, go to (11) if sector count = 0.
(10)	1000-05:	Go to Step (2).
(11)	1000-05:	Activates INTRQ.

WRITE SECTOR

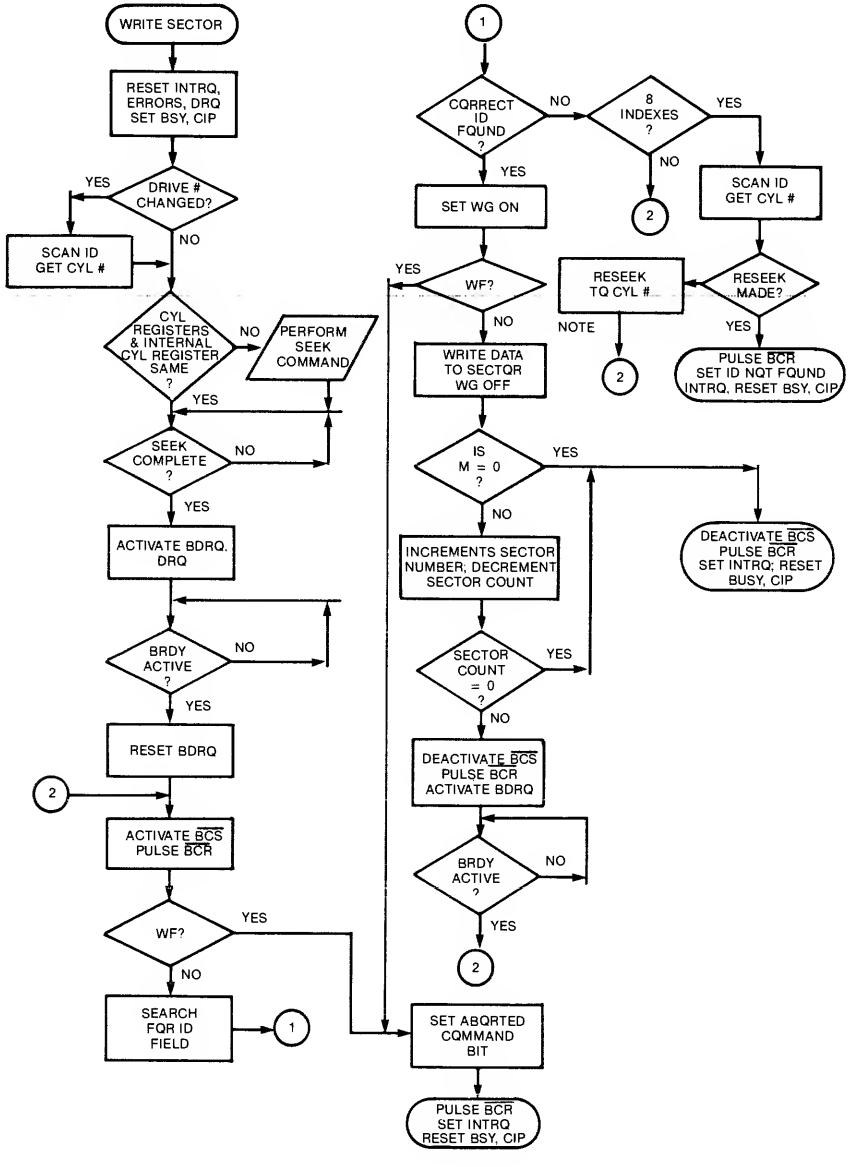
The write sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1000-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a seek command takes place. Write fault and DRDY lines are checked throughout the command.

After Seek complete is found to be true (with or without an implied seek), the BDRQ signal is made active and the host proceeds to load the buffer. When the WD1000-05 senses the BRDY line going high, the ID field with the specified cylinder, head, and sector size is searched for. Once found, the write gate signal is raised and the data is written to the disk. If the ID field cannot be found within 8 revolutions, the ID not found bit is set and the command is terminated.

During a multiple sector write operation (M flag = 1), the sector number is incremented and the sector count register is decremented. If the BRDY line is asserted after the first sector is read out of the buffer, the WD1000-05 will continue to read data out of the buffer for the next sector. If BRDY is inactive, the WD1000-05 will raise BDRQ and wait for the host to place more data in the buffer.

In summary then, the write sector operation is as follows:

(1)	Host:	Sets up parameters; issues write sector command.
(2)	1000-05:	Strobes $\overline{BCR}$; sets BDRQ = 1, DRQ flag = 1.
(3)	Host:	Loads buffer with data (by $\overline{WE}$ strobes).
(4)	1000-05:	Waits for BRDY = low to high.
(5)	1000-05:	Finds specified ID field, write out sector.
(6)	1000-05:	If M = 0, then interrupt; End.
(7)	1000-05:	Increments sector number, decrements sector count.
(8)	1000-05:	If sector count = 0, then interrupt; End.
(9)	1000-05:	If BRDY = inactive, then (5).
(10)	1000-05:	Go to (2).



SCAN ID

The scan ID command is used to update the head, sector size, sector number and cylinder registers.

After the command is loaded, the seek complete line is sampled until true. The ready and write fault lines are also checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, cylinder, and sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, the WD1000-05 will retry up to 8 revolutions to find an error-free ID field. There is no implied seek with this command and the buffer is left undisturbed.

FORMAT

The format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 2 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A H'00' is normal; a H'80' indicates a bad block mark for that sector. In the example of Figure 2, sector 04 will get a bad block mark recorded.

	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
:				:				
:				:				
F0	FF	FF	FF	FF	FF	FF	FF	FF

Figure 2. FORMAT COMMAND BUFFER CONTENTS

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY to tell the WD1000-05 to begin formatting the track.

An implied seek is also in effect on this command. As in other commands, if the drive number has changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incompatible format had been used), an IDNF error will result and the Format command will be aborted. This can be avoided by issuing a Restore command before formatting.

The sector count register is used to hold the total number of sectors to be formatted, while the sector number register holds the number of bytes minus 3 to be used for Gap 1 and Gap 3; for instance, if the sector count register value is 2 and the sector number register value is 0, then 2 sectors are written and 3 bytes of H'4E' are written for Gap 1 and Gap 3.

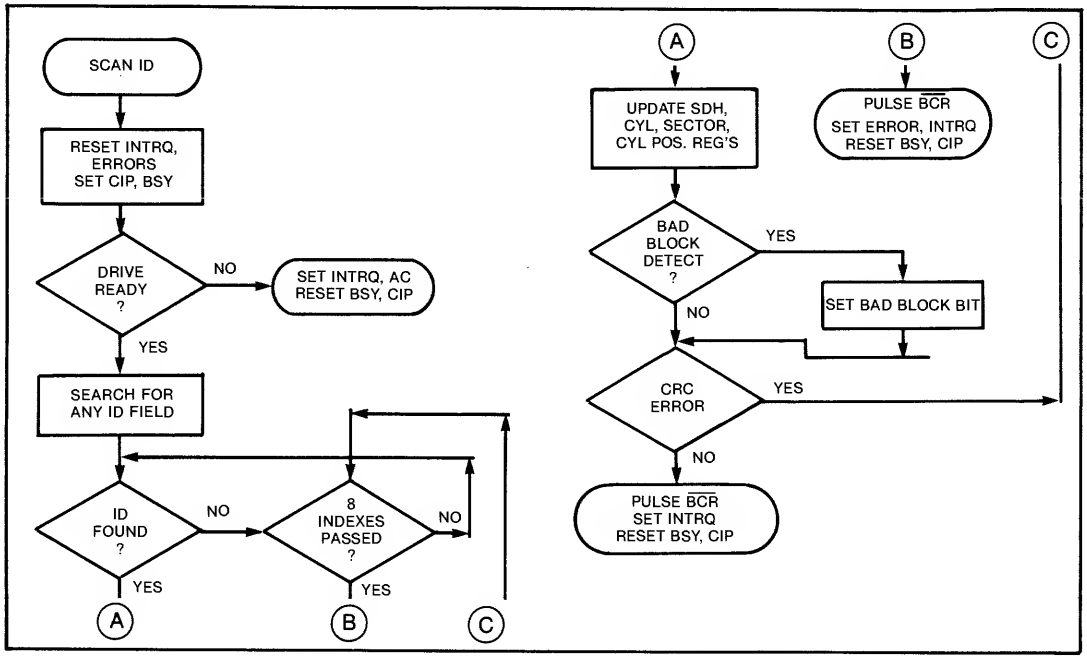
The data fields are filled with H'FF,' and CRC is automatically generated and appended. The sector extension bit of the SDH register should not be set. After the last sector is written, H'4E' is filled until index. Like all commands, a write fault or drive not ready condition will terminate the command. Figure 3 shows the format that the WD1000-05 will write on the disk.

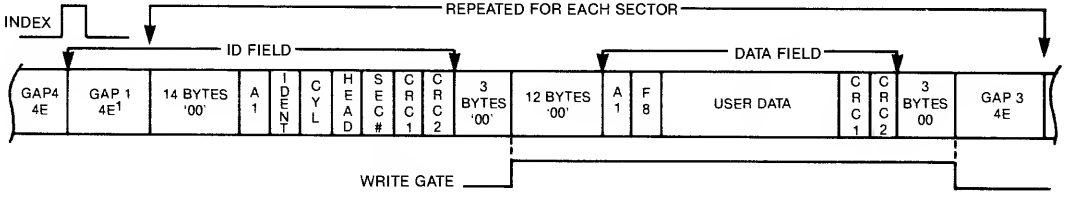
The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining the minimum Gap 3 value is:

Gap 3 = 2*M*S + K + E

M = motor speed variation (e.g. .03 for + − 3%)
S = sector length in bytes
K = 25 for interleave factor of 1
K = 0 for any other interleave factor
E = 7 if the sector is to be extended

Like all commands, a write fault or not ready condition will terminate the command. Figure 3 shows the format that the WD1000-05 will write on the Disk.





ID FIELD

A1 = H'A1' with H'0A' clock.

IDENT = MSB of Cylinder Number
FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512-767 Cylinders
FD = 768-1023 Cylinders

HEAD = Bits 0, 1, 2 = Head Number
Bits 3, 4 = 0
Bits 5, 6 = Sector Size
Bit 7 = Bad Block Mark

Sec # = Logical Sector Number

DATA FIELD

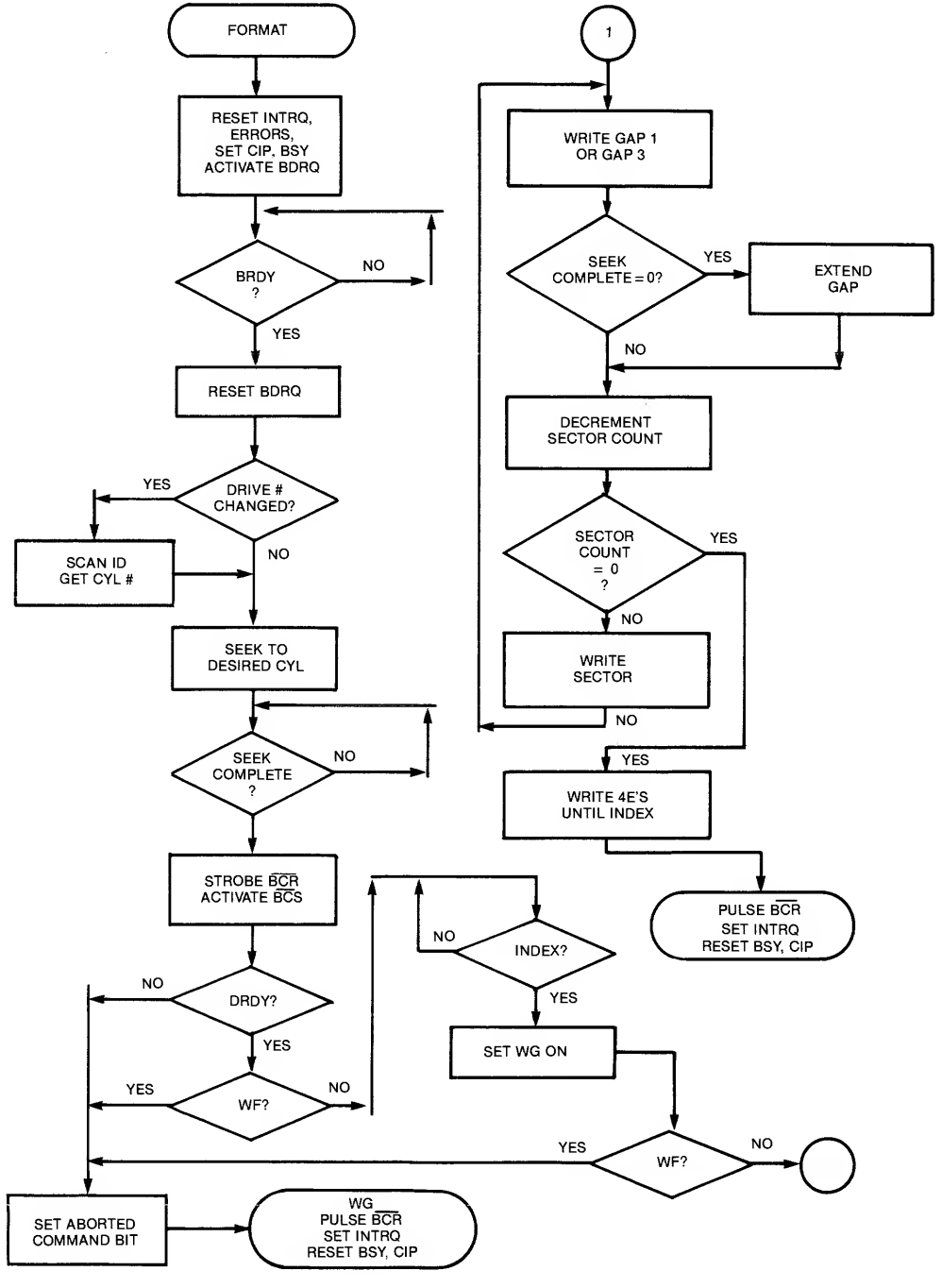
A1 = H'A1' with H'0A' Clock

F8 = Data Address Mark; Normal Clock

USER = Data Field 128 to 1024 Bytes[2]

NOTES:
1. GAP1 and 3 length determined by sector number register contents during formatting.
2. If EXT bit in SDH register is set to 1 then an additional 7 data bytes are written, no CRC bytes are written.

Figure 3. FORMAT


FORMAT
RESET INTRQ, ERRORS, SET CIP, BSY ACTIVATE BDRQ
BRDY ?
NO
YES
RESET BDRQ
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SEEK TO DESIRED CYL
SEEK COMPLETE ?
NO
STROBE BCR ACTIVATE BCS
DRDY?
NO
YES
WF?
YES
NO
SET ABORTED COMMAND BIT
WG PULSE BCR SET INTRQ RESET BSY, CIP
1
WRITE GAP 1 OR GAP 3
SEEK COMPLETE = 0?
YES
EXTEND GAP
NO
DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
WRITE SECTOR
NO
YES
WRITE 4E'S UNTIL INDEX
PULSE BCR SET INTRQ RESET BSY, CIP
NO
INDEX?
YES
SET WG ON
YES
WF?
NO

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

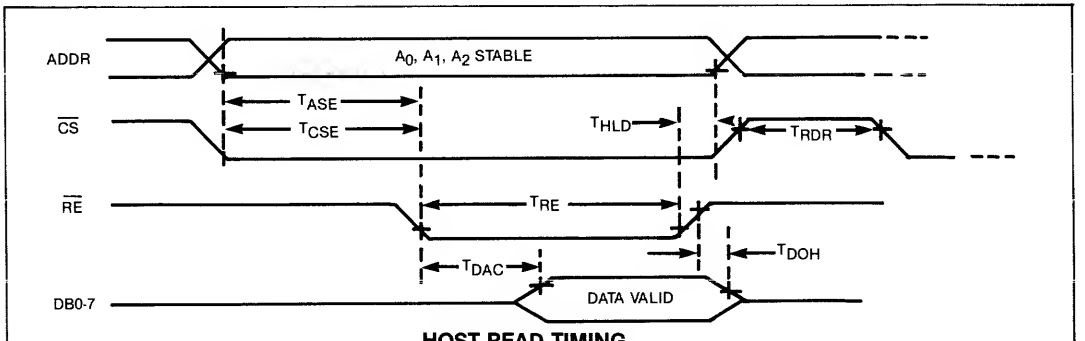
DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		± 10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Draw)		± 10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = −100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
V_{OL}	Output Low Voltage (Pins 21-23)		0.45	V	IO = 4.8 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	For Pins 25, 34, 37, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise Time		30	ns	10% to 90% points

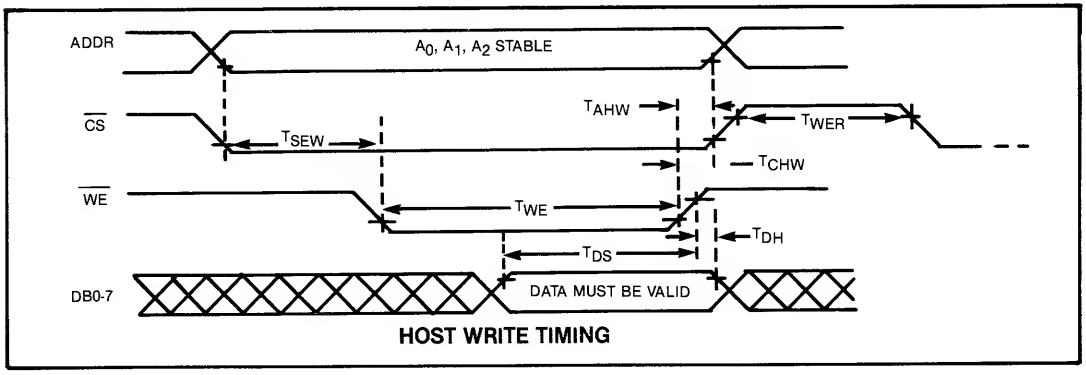
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{ASE}	ADDR Setup to $\overline{RE}$	100		ns	
T_{DAC}	Data Valid from $\overline{RE}$		375	ns	
T_{RE}	Read Enable Pulse Width	.4	10	μs	
T_{DOH}	Data Hold from $\overline{RE}$	20	200	ns	
T_{HLD}	ADDR, CS, Hold from $\overline{RE}$	0		ns	
T_{RDR}	Read Recovery Time	300		ns	
T_{CSE}	$\overline{CS}$ Setup To	0		ns	



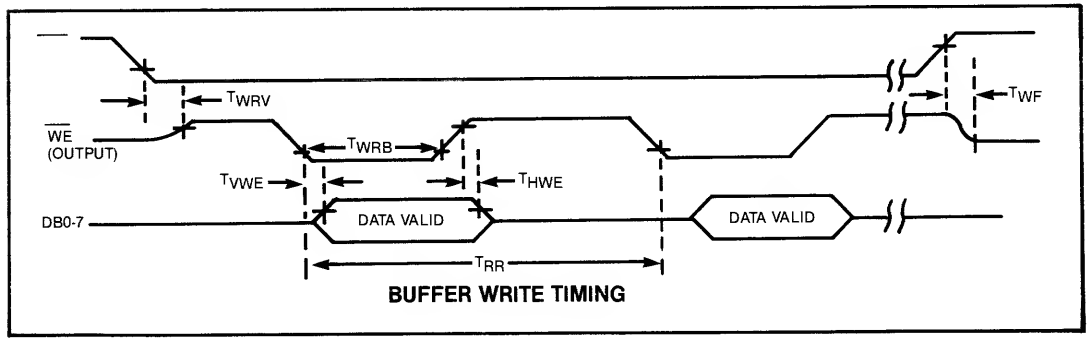
HOST READ TIMING



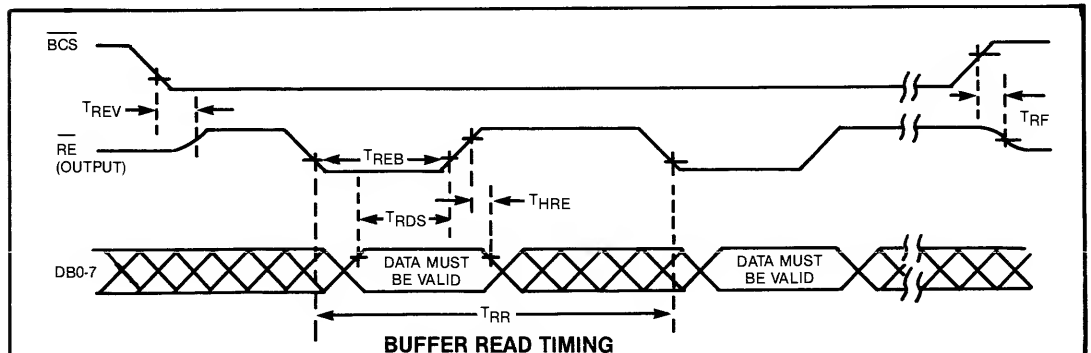
HOST WRITE TIMING

HOST WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SEW}	ADDR, CS Setup to $\overline{WE}$	0	10	µs	
T_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	µs	
T_{WE}	Write Enable Pulse Width	.2	10	µs	
T_{DH}	Data Bus Hold from $\overline{WE}$	10		ns	
T_{AHW}	ADDR Hold from $\overline{WE}$	30		ns	
T_{WER}	Write Recovery Time	1.0		µs	See Note 1
T_{CHW}	$\overline{CS}$ Hold Time	0			



BUFFER WRITE TIMING



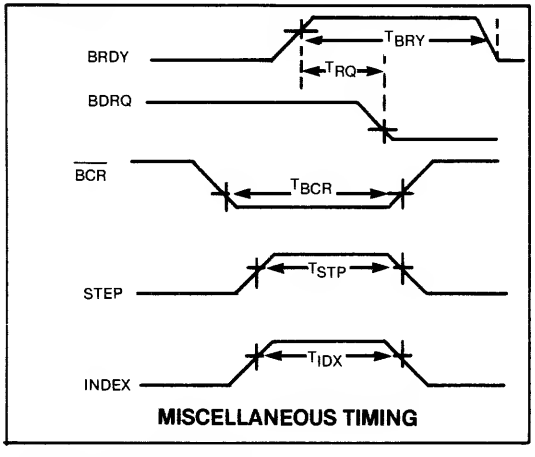
BUFFER READ TIMING

BUFFER WRITE TIMING (READ SECTOR CMD)

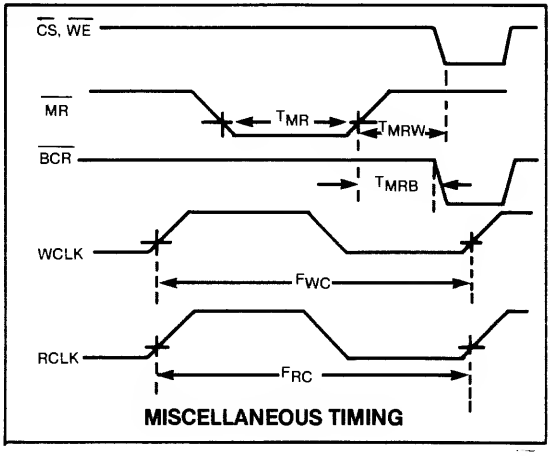
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	ns	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{VWE}	Data Valid from $\overline{WE}$			110	ns	
T_{HWE}	Data Hold from $\overline{WE}$	60			ns	
T_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	µs	See Note 2
T_{WF}	$\overline{WE}$ Float from BCS	15		100	ns	C_L = 50 pf

BUFFER READ TIMING (WRITE SECTOR CMD)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	ns	C_L = 50 pf
T_{REB}	$\overline{RE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{RDS}	Data Setup to $\overline{RE}$	140			ns	
T_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	µs	See Note 2
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	ns	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			ns	



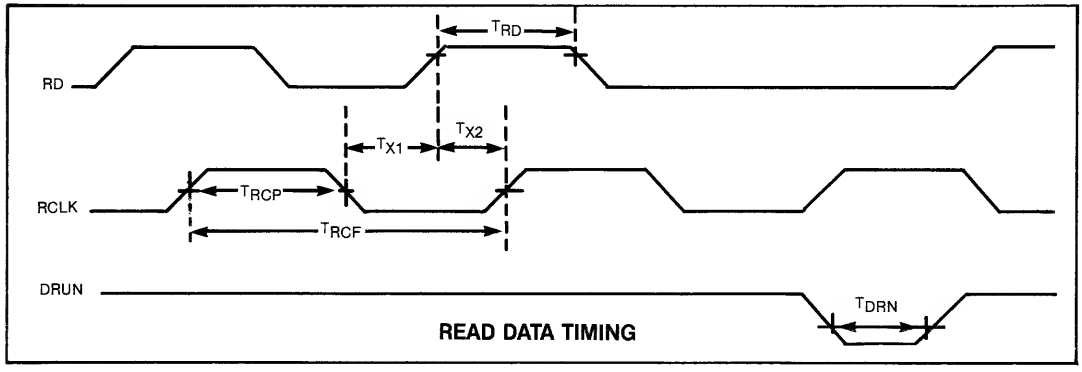
MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

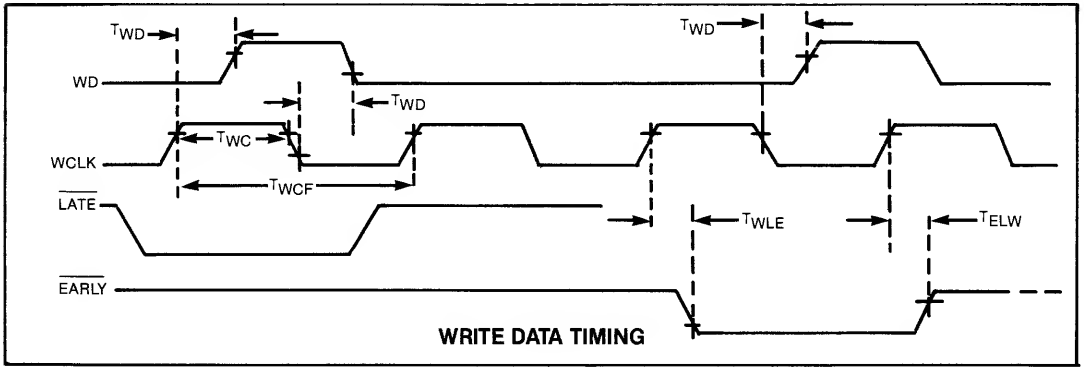
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RQ}	BDRQ Reset from BRDY	40		200	ns	
T_{BCR}	Buffer Counter Reset Pulse Width	1.4	1.6	1.8	µs	See Note 2
T_{STP}	Step Pulse Width	8.3	8.4	8.7	µs	See Note 2
T_{IDX}	Index Pulse Width	5		15	µs	
T_{MR}	Master Reset Pulse Width	24			WC	See Note 3
F_{WC}	Write Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
F_{RC}	Read Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
T_{BRY}	BRDY Pulse Width	800			ns	See Note 5
T_{MRB}	$\overline{MR}$ Trailing To $\overline{BCR}$	1.6	3.2	6.4	µs	See Note 2
T_{MRW}	$\overline{MR}$ Trailing To Host Write	6.4			µs	See Note 2



READ DATA TIMING

READ DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	95		2000	ns	50% Duty Cycle
T_{X1}	RD from RCLK Transition	0		$T_{RCP} \div 2$	ns	
T_{X2}	RD to RCLK Transition	20		$T_{RCP} \div 2$	ns	
T_{RD}	RD Pulse Width	40		T_{RCP}	ns	
T_{DRN}	DRUN Pulse Width	30			ns	
T_{RCF}	RCLK Frequency	.250		5.25	MHZ	See Note 6



WRITE DATA TIMING

WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	ns	
T_{WD}	Prepagation Delay WCLK to WD	10		65	ns	
T_{WLE}	WCLK to Leading Early/Late	10		65	ns	
T_{ELW}	WCLK to Trailing Early/Late	10		65	ns	
T_{WCF}	WCLK Frequency	.250		5.25	MHZ	See Note 6

NOTES:
1. AC timing measured at $V_{OH} = 2.0V$, $V_{OL} = 0.8V$, $C_L = 50$ pf.
2. Based on WCLK = 5.0 MHz.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz).
4. 2 WCLK ± 100 ns.
5. BRDY must be >4 μs or a spurious BDRQ pulse may exist for up to 4 μs after rising edge of BRDY.
6. $T_{RCF} = T_{WCF} \pm 15\%$.

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